Photon imaging using post-processed CMOS chips

Joost Melai

The graduation committee consists of:

Chairman:	Prof. Dr. Ir. A.J. Mouthaan	University of Twente
Secretary:	Prof. Dr. Ir. A.J. Mouthaan	University of Twente
Promotor:	Prof. Dr. J. Schmitz	University of Twente
Ass't promotor:	Dr. Ir. C. Salm	University of Twente
Members:	Prof. Dr. K. Desch	University of Bonn
	Dr. Ir. H. van der Graaf	Nikhef, Amsterdam
	Prof. Dr. M.C. Elwenspoek	University of Twente
	Prof. Dr. Ir. R.A.M. Wolters	NXP Semiconductors and University of Twente
	Prof. Dr. G. van der Steenhoven	University of Twente

This research was supported by Dutch Technology Foundation STW (Project TET 6630: "There's plenty of room at the top") and carried out at the Semiconductor Components group, MESA+ Insititute for Nanotechnology, University of Twente, The Netherlands.

The cover shows images of UV light recorded with a Timepix chip (chapter 5). To do this an InGrid detector structure and a CsI photocathode have been post-processed onto the IC.
The background that is used on the cover is an image of patterns in porous alumina, a material that has been investigated for the structures described in chapter 6.

PhD thesis – University of Twente, Enschede, the Netherlands

Title: Photon imaging using post-processed CMOS chips

Author: Joost Melai

ISBN: 978-90-365-3132-0

DOI: 10.3990/1.9789036531320

© 2010 Joost Melai

PHOTON IMAGING USING POST-PROCESSED CMOS CHIPS

PROEFSCHRIFT

ter verkrijging van
de graad van doctor aan de Universiteit Twente,
op gezag van de rector magnificus,
prof. dr. H. Brinksma,
volgens besluit van het College voor Promoties
in het openbaar te verdedigen
op dinsdag 21 december 2010 om 15.00 uur

door

Joost Melai

geboren op 30 december 1976
te Nijmegen, Nederland

This dissertation is approved by:
Prof. Dr. Jurriaan Schmitz (promotor)
Dr. Ir. Cora Salm (supervisor)

To Eefje

Contents

Preface **1**

1 Introduction **3**
1.1 Integrated photon detector concepts 4
1.1.1 Solid-state photon detectors 4
1.1.2 Vacuum operated photon detectors 8
1.1.3 Gaseous photon detectors 11
1.2 Experimental work on integrated photon detectors 15
1.2.1 Integrated Micromegas for photon detection 15
1.2.2 Integrated MCP for photon detection 16
1.3 SU-8 as a construction material 16
1.3.1 Standard SU-8 process 17
1.3.2 SU-8 characterization 18

2 Dielectric strength of SU-8 **19**
2.1 SU-8 in High-Voltage applications 19
2.2 Experimental details 20
2.2.1 Electrical test structures 20
2.2.2 Processing of test structures 20
2.2.3 Electrical characterization 23
2.3 Results and discussion 25
2.3.1 Low-field conduction 25
2.3.2 Conduction mechanism 26
2.3.3 Dielectric strength 29
2.3.4 Influence of Hard-Bake steps on the dielectric strength of SU-8 32
2.4 Conclusions 34

3 Outgassing from SU-8 **35**
3.1 Experimental methods 36

3.2 Results and discussion 37
3.2.1 Mass spectrometry measurements 37
3.2.2 GC-MS measurements 39
3.3 Conclusions 44

4 Photon sensitive InGrids: detector design 47
4.1 The detector system 47
4.2 The Timepix CMOS imaging chip 48
4.2.1 Initial post-processing of the chips 50
4.3 The InGrid structure 50
4.4 InGrid geometry 52
4.5 Detector integration and operation 57
4.6 The CsI photocathode 60
4.6.1 Wavelength dependence 63
4.7 Measurement methods 63
4.7.1 Pulse measurements with chip based detectors 64
4.7.2 Test devices with a single anode 64
4.7.3 Gas choice 65
4.8 Summary 67

5 Photon sensitive InGrids: experimental results 69
5.1 Photon detection without a dedicated photocathode 69
5.2 Results with single anode detectors 71
5.2.1 Current mode measurements 72
5.2.2 Pulse measurements 76
5.3 Results with chip based detectors 78
5.3.1 Gain as determined from pulse measurements 79
5.3.2 Spectra with and without CsI 81
5.3.3 Using the TOT count to establish bias dependencies . . 84
5.3.4 Spatial resolution using the slanted edge method 86
5.3.5 Imaging results 88
5.4 Conclusions 88

6 Towards integrated MCPs 91
6.1 MCP principle of operation 91
6.1.1 Gain model and simulation results 92
6.1.2 Choice of the geometry 94
6.2 Al_2O_3 MCP structures 97
6.3 SU-8 MCP structures 99
6.4 Conclusions 102

Conclusions and recommendations **105**

Samenvatting **109**

Acknowledgement **111**

About the author **113**

Bibliography **115**

Preface

This thesis presents our work on an integrated photon detector made by post-processing of CMOS sensor arrays. The aim of the post-processing is to combine all elements of the detector into a single monolithic device. These elements include a photocathode to convert photon radiation into electronic signals (in the extreme case this conversion is from a single photon into a single electron), an electron multiplication structure to increase the magnitude of the signal pulse and a position sensitive recording element to register the place, time and size of the electron charge pulse. The recording element is part of a CMOS imaging IC. The rest of the detector structure is processed directly onto the CMOS substrate. This method is called post-processing.

It is essential that the post-processing steps that are used are compatible with the underlying CMOS devices. The process should not harm the IC or change the functionality in any way. Ideally none of the elements of the IC are affected and the IC behaves exactly as non-postprocessed copies. Only then the CMOS design can be used in the exact same way without any need for design variations or remodeling. The work presented in this thesis fits in a larger project focused on post-processing of CMOS substrates called 'There's plenty of room at the top'. This project is, at the time of writing, in its final stage at the Semiconductor Components group of the University of Twente.

Outline

The first chapter contains an overview of photon detection methods. Two types of photon detectors are investigated experimentally. These are an integrated gaseous multiplication detector (InGrid, with a so called Micromegas layout) and a device that uses vacuum operated electron multiplication (a Micro Channel Plate or MCP). The technological methods used to fabricate these structures are discussed briefly. In a large part of the experimental work SU-8 is used as a construction material; we will introduce this material also in the first chapter.

Chapter 2 and 3 discuss different material aspects of SU-8 that are important for the use in detectors. The chapters deal with the dielectric strength of SU-8 and outgassing from SU-8, respectively. Both topics have not previously been documented in scientific literature, despite the fact that the investigated material properties are important in many different application areas. It appears that for most researchers the material (SU-8) simply fulfills their needs. Although both of these chapters do not provide a final exhaustive characterization we do believe they show significant progress in these areas, the findings can be useful for many fields.

Chapter 4 deals with gaseous detection structures for the use in photon detection. The InGrid detector is introduced, the technology to fabricate it and its operation are discussed. Special emphasis is given to the addition of a photocathode to make the structure photon sensitive. The resulting device is the first fully monolithic embodiment of a high resolution UV-photon imaging detector.

The next chapter, No. 5, reports results from photon detection experiments with various InGrid devices with and without CsI photocathodes.

Chapter 6 discusses the possible use of MCP-like structures in an integrated, monolithic, CMOS based photon detector. Several methods to make such a structure are discussed. These structures have not been successfully fabricated, this chapter therefore mainly leads to suggestions for further research rather than tangible results or hard conclusions.

The final chapter contains conclusions and recommendations that can be made based on the research work presented here.

Chapter 1

Introduction

There are many types of photon detectors, from solid-state detectors to vacuum operated Photo Multiplier Tubes. The majority of photon detectors rely on the photoelectric effect. A photon excites an electron of one atom in a solid target and, if the photon energy is sufficient, the electron is emitted. The photoelectron is extracted from and directed away from the surface by an appropriate electric field. The photoelectron charge can be detected directly or it can first be multiplied to enhance sensitivity. There are also other methods of photon detection. In bolometry the energy that is adsorbed after photon capture is sensed and used as a measure for illumination. Chemical detectors such as photographic film rely on the change in material parameters after exposure to radiation.

In this thesis we are focussing on integrated detectors, meaning that all detector elements are combined into one monolithic device. Furthermore the interest is narrowed to imaging detectors. This means the readout structure that is used is capable of recording the arrival location in a 2D plane. This is most easily achieved by using a pixelized detector plane, apart from location these detectors can potentially also record arrival time. Each pixel acts as a single independent detector.

Choosing the right detector for a certain application depends on many aspects. Important performance indicators are the efficiency (how many of the photons are detected), the sensitivity (how few photons can be detected, ideally a single photon) and the maximum rate speed at which individual events can be distinguished. One important geometrical aspect is the segmentation, defined by how small the detector elements can be made and how close they can be packed. It has a big influence on the resolution that can be attained. Another aspect is the total sensitive array size that can be achieved, for some applications very large detector planes are needed. Furthermore there are operational requirements to consider such as power consumption, high voltage, gas supply, cooling and vacuum. For specific purposes it might be important to consider the impact on detector performance of

environmental conditions such as magnetic fields, radiation (other than photons) or vibrations. However, we will not go into these special conditions here.

1.1 Integrated photon detector concepts

The detectors that we focus on have a solid photocathode that converts photons into photoelectrons, a multiplication structure that multiplies the created charge signal into a measurable amount and a readout structure. Other detectors, such as photodiode arrays, combine the last two or all three of these functions in a single component.

The charge multiplication can be performed in several ways, in solid-state media, by interaction of electrons accelerated in vacuum with solid matter and by interaction of accelerated electrons with gas. These three concepts are discussed in the following sections.

1.1.1 Solid-state photon detectors

Solid state photo cathodes are made using semiconductor technology. This allows the detectors to be made with a very small pitch. In other words, a high granularity can be reached. The maximum substrate size is for most technologies limited to 8″ wafers. However, Canon Inc. has recently announced a 202×205 mm^2 CMOS imaging array, this single device just fits onto a 12″ wafer [1]. Larger detector areas can be made by tiling elements [2]. A good example of a very large tiled detector array is shown in fig. 1.1.

When detectors are tiled a certain amount of space is needed for connections, at least on one side of the substrate. This region will not be sensitive. A solution to this is to provide connections from the backside, where the infrastructure can be made without extending beyond the projected size of the sensitive area. This requires connections from the front side to the backside of the detector substrate as well as many other advanced technologies, for instance related to edge termination of the detector bias voltage. Examples of such a tiled detector can be found in [4].

The sensitive element in solid-state photon detectors is a semiconductor. Photons convert in the semiconductor and the charge is detected. When a photon strikes an atom in the semiconductor lattice with sufficient energy a free, so called interstitial, electron can be generated. At the same time a positive charge is created at the vacated lattice site. Other electrons can move to there, making the gap act as a positive mobile charge carrier (referred to as a hole). As a result of the photon impact an electron-hole pair is generated. When there is an electric field applied in the semiconductors the positive and the negative charge can be separated, each drifts to opposite sides of the material. The moving charge can be detected with sensitive electronic components, either simply as current or with more advanced

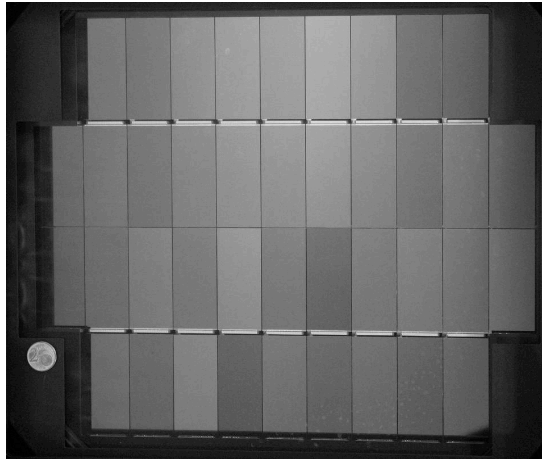

Figure 1.1 – *The MegaPrime CCD mosaic of 40 CCDs with in total 380 MPixels, this array is used in the Canada-France-Hawaii telescope [3].*

electronic circuits where the charge is measured by having it alter the bias point of one branch of a current mirror.

Integrated photon detectors are combined with active electronics for readout and signal processing, ideally in a single, monolithic system-on-chip. The most important technology for such active devices is CMOS technology. Given the use of silicon the sensitivity to radiation with an energy corresponding to less than the bandgap (1.2 eV at room temperature) will be poor, this corresponds to a wavelength of 1.2 μm. The material sensitivity extends to deep UV radiation. In the visible range of light the conversion efficiency can be close to 100% [5].

For monolithic detectors a trade-off has to be made in the material (purity, doping distribution) and processing aspects for optimization of both the CMOS structures as well as the detector structures. Another trade-off is found in the use of available areal space. Peripheral electronics limit the sensitive area for a given detector size. To prevent this it is possible, at the cost of increased complexity and price, to couple a CMOS readout element to a separate dedicated detector photodiode array. The two dies are interconnected using bumpbonding. The detector die can be a thick Si substrate [6] or it can be made out of compound semiconductor materials (with higher Z and therefore higher stopping power) such as GaAs [7] or CdTe [8]. These detectors are called Hybrid Pixel Detectors (HPDs), we will not consider them further as they are not monolithic integrated detectors.

The charge coupled device (CCD)

One of the most common semiconductor imaging detectors is the Charge Coupled Device or CCD [9, p. 697]. The device has been invented at Bell Labs.

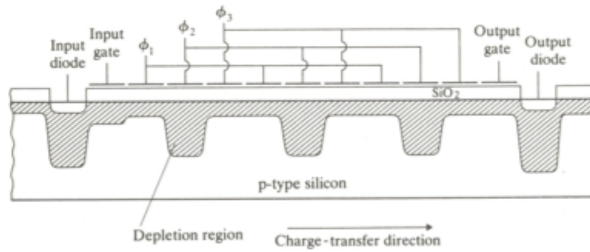

Figure 1.2 *– Illustration of a CCD with three capacitors per pixel, taken from [11]. In this example there are only three pixels.*

Willard Boyle and George Smith have received the 2009 Nobel prize in physics for their work on the physical principles of CCD operation [10]. The CCD consists of an array of MOS capacitors made into (typically) an epitaxial layer. Figure 1.2 shows an example of such an array. Charge is created in the epitaxial layer during exposure by photoexcitation. The gates of all the MOS capacitors can be addressed externally.

The biasing can be changed such that charge will move from one gate to the next. This is achieved by first equalizing the potential of gate n+1 to that of gate n. Charge, accumulated under gate n, will spread over the two capacitors. The biasing is then altered so that gate n+1 attracts all the charge as it is pushed away from gate n. The biasing scheme is illustrated in fig. 1.3. In this manner charge can be shifted across the array; the mechanism is somewhat similar to the action of a peristaltic pump.

If each pixel contains a number of capacitors, at least 2, normally 3 or 4, the charge signals of different pixels can be kept separated. The charge is read out by moving it along the columns of the array towards the end where charge sensitive amplifiers convert the measured charge to voltage pulses. These pulses can be converted to a digital signal and this bit stream can be recorded with a digital circuit in the periphery of the device.

The peripheral electrodes are made using standard CMOS processing, the CCD itself requires some additional processing that is not standard but compatible with normal CMOS processing. As a result process complexity and cost are higher than for plain CMOS. The doping distribution and thickness of the epitaxial layer can be tailored to increase sensitivity to the incoming radiation.

An additional improvement to CCD is made with the Electron Multiplying CCD (EMCCD) [13]. In this device avalanche multiplication is used to enhance the initial charge to increase the sensitivity. This is similar to the Avalanche Photo Diode (APD) discussed below.

Spontaneous generation of charge carriers in the sensitive layer can lead to

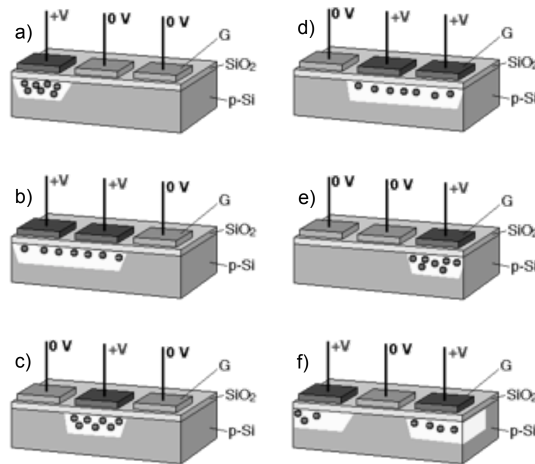

***Figure 1.3** – Simplified illustration (from [12]) of the biasing mechanism used to transfer charges across the capacitor elements of a CCD. In this example each pixel has three capacitors. Going from a) to f) the bias voltage is cycled in three phases to manipulate the charge.*

significant dark current. This means that for sensitive detectors the generation needs to be limited by careful control of material purity of the epitaxial layer and by cooling. With sufficient cooling (below -60 °C) CCDs can be made single photon sensitive [14].

Photodiode arrays

An older semiconductor detector is the photodiode [9, p. 671]. Light falls onto a semiconductor body that is part of a diode, changing the diode characteristics. A normal mode of operation is to slightly reverse bias the diode. Photons that convert in the diode depletion region will create charges that will increase the diode current. This photocurrent is proportional to the photon flux. If such photodiodes are made into an array it can be used for imaging. If the passive photodiode is coupled to an active CMOS readout element in each pixel we speak of an Active Pixel Sensor [15]. The diode is made directly in CMOS technology requiring hardly any process changes, the possibilities for larger arrays with finer pitch therefore follow continuing advances in scaling of CMOS devices. In an APS each pixel contains more electronics than in a CCD array (where readout is only performed on the periphery). The added pixel complexity requires space, this means less of the total detector area can be used for effectively sensing photons. Having an array of amplifiers means signals can be processed much faster, detector dead time during readout can be much lower. Variations from pixel to pixel do mean that

the device needs more careful calibration.

The signal-to-noise ratio of a detector system determines the minimum amount of photons that can be detected. For low photon flux the performance of the detector is limited by shot noise. Charge sensing electronics typically require a signal of 10^3–10^4 electrons [15]. This means we can not simply detect single photons. To extend the performance towards single photon sensitivity the initial signal (a photoelectron) needs to be amplified into a larger charge. This can be done by increasing the reverse bias across the photodiode. The sensitive area, the depletion region of the diode, is made wide by incorporating a thick lowly doped or near-intrinsic region in the diode. This layer is fully depleted. When an electron-hole pair is generated by a photon the charge carriers are moved towards the ends of the depletion region, just as in a conventional photodiode. However, if the depletion region is wide enough and the applied bias voltage is high enough the drifting electrons acquire so much energy that, when they collide with the Si lattice, the energy is sufficient to generate further charge carriers through impact ionization. These secondary electrons are also accelerated by the electric field. An avalanche process is initiated, leading to the creation of a much larger charge cloud. This large signal can be easily detected by the CMOS circuit. Because avalanche multiplication is used to boost the initial photoelectron signal such a device is then called an Avalanche Photo Diode (APD). Examples of such detectors are presented by Zappa *et al.* [16, 17], Kindt *et al.* [18] and Rochas *et al.* [19]. Rae *et al.* [20] show a hybrid system containing Single Photon Avalanche Diodes (SPADs) for the detection of light from fluorescent material in biodiagnostics. If an APD is made sufficiently sensitive to reliably detect single photons it is sometimes referred to as a silicon photo-multiplier, or SiPM [21].

Postprocessed photodiode arrays

The photodiode array can also be post-processed onto a CMOS imaging array. References [22, 23, 24] present such devices. They consist of an amorphous Si photodiode array that is post-processed onto a CMOS charge sensitive imaging chip. The devices in [22, 23] have been made by using Very High Frequency Plasma Enhanced CVD (VHF-PECVD); the amorphous Si can then be deposited at temperatures that are compatible with the CMOS readout chip. Other semiconductive layers can also be post-processed, reference [25] shows a $CuInGaSe_2$ thin film image sensor that is deposited on top of a CMOS imaging array.

1.1.2 Vacuum operated photon detectors

The Photo-Multiplier (PM) tube

The most common single photon sensitive detector is the Photo-Multiplier (PM) tube. Figure 1.4 contains an illustration of a typical PM.

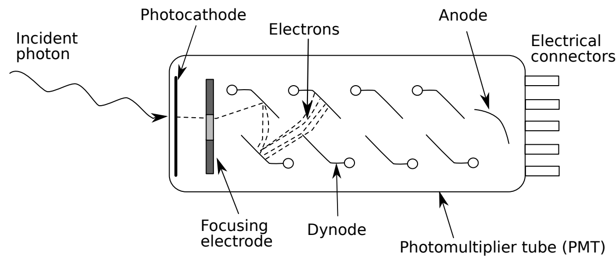

***Figure 1.4** – Illustration of a PhotoMultiplier Tube (PMT), (adapted from [26]). This example has 8 dynodes, most PMTs have at least 12 stages.*

It consists of a cylindrical vacuum chamber with an entrance window on one side, a photocathode is deposited on the inner surface of the window. In this layer incoming photons convert into a photoelectron which is emitted and then drifts further into the tube driven by the electric field applied to the structure. The electron collides with a solid metal electrode (called a dynode) that is mounted on the tube sidewall. The impact generates secondary electrons through impact ionization. The secondary electrodes are again accelerated towards a next dynode. A typical PM tube has 12–15 dynodes placed along the tube, biased with higher and higher positive voltage. At the other end of the detector the avalanche charge cloud is detected using an anode that can be connected to a charge sensitive amplifier. The amplification can be so large (10^5–10^7) that even a single photon can be detected with good efficiency. The tricks of the trade are in the vacuum and the dynode material. The former is needed to allow electrons to gather enough kinetic energy for the following ionization as well as to prevent degradation of the photocathode. The latter is to ensure good secondary electron yield. The dynodes are often coated with thin dielectric layers that enhance the generation of electrons. PMs are very sensitive but they are large structures that are difficult to pack together closely. This makes them unsuitable for imaging purposes, except for very large detectors. One such example is the Super Kamiokande experiment [27]; it consists of an array of more than 11000 large PMTs (50 cm in diameter) that surround a tank of ultrapure water of 41 m in height and 39 m in diameter. The imaged photons are emitted in the water, as so called Čerenkov radiation, after the conversion of neutrinos. The detector can be used for particle physics (such as the study of neutrino properties or proton decay) as well as for astronomy and astrophysics.

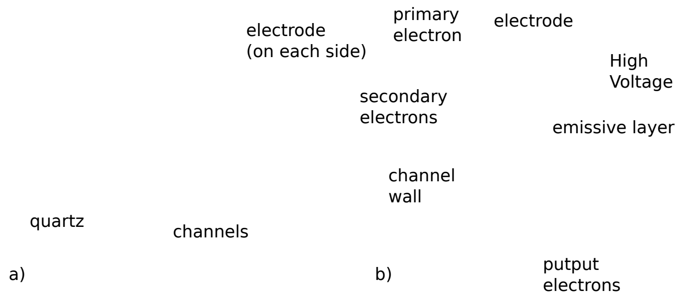

__Figure 1.5__ – Illustration of a) an MCP and b) a single pore and its operation principle. This figure is taken from [28].

MCP based detectors

Another vacuum operated detector is based on the use of a Micro Channel Plate (MCP) [28] coupled to a photocathode. MCPs are thin disks with straight pores running from one face to the other, as illustrated in fig. 1.5a. A large bias voltage is applied across the disk. The two faces of the disk are usually metallized but the disk itself is made out of a dielectric material such as quartz glass. Electrons enter the structure from above and are accelerated into a pore, when they collide with the sidewall secondary electrons are created. These are in turn accelerated and cause impact ionization, leading to an avalanche multiplication process along the length of the pore, as shown in fig. 1.5b. The MCP pore can be viewed as a PM tube with one distributed dynode. The sidewall of the pore is engineered not only to have good secondary electron yield on impact ionization but also for distribution of the bias voltage: the pore sidewalls act as a distributed resistor. The resistance is tuned to have an acceptable leakage current while still providing good supply to replace extracted electrons.

CCDs are commonly combined with MCPs (and photocathode) to create a highly sensitive imaging system. These systems are known as Image Intensified CCDs. They are used for many applications ranging from science [29] to night vision equipment [30].

Hybrid vacuum and solid-state detectors

Another option to improve CCD performance is to supply a higher energy to the charge detected by the imager. This is done in the Electron Bombarded CCD (EBCCD), see for instance [31] for an application of this technique for imaging. Photons are first converted into photoelectrons with a photocathode, mounted above the CCD at some distance. The emitted photoelectron is accelerated towards the CCD, in vacuum, due to a high applied bias potential (> 10 kV). When a photoelectron strikes the CCD surface it does so with considerable energy. This

releases a significant charge (several thousands of electrons) which can be detected by the imaging array. The readout can also be achieved with a photodiode array, for instance in the Hybrid Photo Detector (HPD, not to be confused with the detectors with the same acronym discussed in section 1.1.1) presented in [32].

John Vallerga and coworkers have coupled MCP electron multipliers to Medipix CMOS imaging chips to provide a system for single photon imaging for astronomy [33, 34] as well as other applications [35]. This detector is not integrated. The CMOS imaging chip is mounted onto a frame and a discrete MCP is mounted above the chip.

1.1.3 Gaseous photon detectors

Similar to the APD or the MCP avalanche multiplication can also be achieved in other media. One type of detector that lends itself particularly well to integration with electronic readout structures is the gas avalanche multiplying detector. There are many of these detectors, but in all cases there are two or more electrodes that supply a high electric field across a volume of gas. Electrons enter the high field region and are accelerated. Charge multiplication occurs when an electron collides with a gas atom and multiple secondary electrons are created. The successive ionization steps result in what is called (gas) avalanche multiplication. A more detailed description can be found in for instance [36, sec. 5] and [37]. When the charge output is a linear function of the detected primary charge we speak of a proportional counter. If the bias voltage between the electrodes is increased further a small input charge results in a large exponential increase in signal. This is called the Geiger regime; in this mode single quanta can be detected and counted as long as the arrival rate is sufficiently low to differentiate events.

These detectors are normally sensitive to free electrons, but they can be used to detect various kinds of radiation. The gas medium itself can be used as a target to detect ionizing radiation. If the detector is coupled to a photocathode photons can be detected by transporting the photoelectrons into the electron detector using a drift field.

Wire detectors

The most well-known gaseous detector is the Geiger-Müller (GM) tube [38]. An anode wire is placed inside a cylindrical gas volume enclosed by a cathode. A high voltage is applied between the two electrodes. Ionizing radiation that crosses the gas volume creates initial electrons in the gas. This signal is amplified, in Geiger mode, and collected by the anode wire. The GM tube detects the passing of individual ionizing particles; these events can be recorded with external electronics. The left panel of fig. 1.6 illustrates the operational principle of the GM counter.

The first and most successful detector capable of determining position and

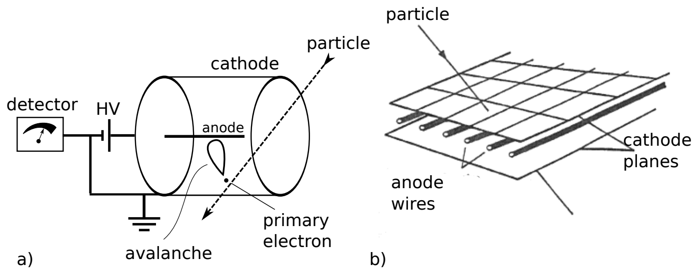

Figure 1.6 – a) A Geiger-Müller (GM) tube and its operational principle and b) a Multi Wire Proportional Chamber (MWPC) (the last image is taken from [39]).

charge of an electron cloud is the Multi Wire Proportional Chamber (MWPC) [40]. It was invented by Georges Charpak of CERN, for which he was awarded the 1992 Nobel Prize in Physics [39]. Wires are stretched across a flat chamber, the wires act as anodes, counterelectrodes are placed above and below the row of wires. Radiation passes the space between the cathodes and initial charge created here is amplified by avalanche multiplication as it travels to the nearest anode wire. The multiplied charge signal is collected by the wires and read out using external amplifiers. The wire chamber can also be made with a photocathode replacing one of the cathode planes, in this way the detector can become photon sensitive. A simple MWPC can only detect location in one direction (perpendicular to the wires). Full 2D imaging can be achieved using multiple MWPC layers or by using a segmented cathode layer to detect the signal from positive ions that are also created during gas ionization.

GEM detectors

Another invention made at CERN is the Gaseous Electron Multiplier (GEM) [41], by Fabio Sauli (1996). It consists of a sheet of a dielectric material (usually a polyimide such as Kapton) cladded with copper on both sides. The assembly is pictured in fig. 1.7. There are holes made through all layers. A bias voltage is applied between the two sides of the detector. Avalanche multiplication occurs in the high electric field inside the hole, across the thickness of the dielectric. The incoming electron signal enters from one side, the readout anode plane is placed on the other side. The electric fields above and below the detector are optimized for efficient transfer. A single GEM foil can only reach limited amplification factors (10^2–10^3). The GEM detector can also be cascaded to provide larger multiplication factors.

Conventional GEMs have a thickness and hole size in the order of 50 μm, they

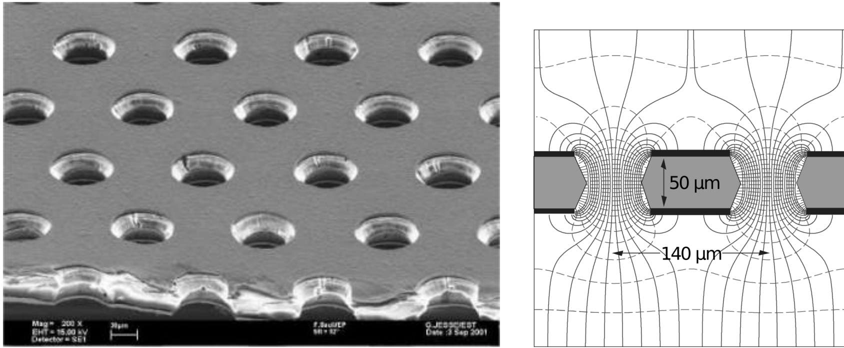

***Figure 1.7** – An SEM image of a GEM foil from CERN (left) and the electric field distribution around it (right). Both images are from the CERN GDD group.*

are made using microtechnology methods such as lithography and etch. Thicker GEMs (THGEMs) are made using modified PCB manufacturing steps (drilling of through-holes and additional etching) out of PCB material. These can be used to create large area detectors. Breskin *et al.* work on such detectors coupled to photocathodes to create large area detectors capable of detecting single photons [42, 43, 44].

Many more variants of GEM detectors exist. There are GEM detectors with resistive electrodes, to prevent sparks [45, 46]. Other systems contain special patterns integrated into the last stage of a multi-GEM stack [47, 48]. These can be used for readout or to capture positively charged ions that are created in the multiplication process. These ions can be detrimental to the photocathode if they drift upwards through the detector stack and reach the photocathode.

Micromegas detectors

A third gaseous detector that can be used for imaging applications is the MicroMesh Gaseous (Micromegas) detector [49], it was invented by Y. Giomataris and G. Charpak. Micromegas consists of a perforated metal foil that is suspended above the anode plane with isolating pillars, placed in a gas ambient. A high electric field is applied in the region below the metal mesh. Initial electrons enter the structure through the holes (from the top), an avalanche occurs on the way towards the anode. The resulting charge cloud hits the anode plane where it is detected. Such a detector can be constructed in many ways. Initial versions where made with a discrete metal mesh and dielectric spacers such as nylon wires or studs placed between the mesh and the anode plane. In later versions the spacers were defined onto the mesh structure.

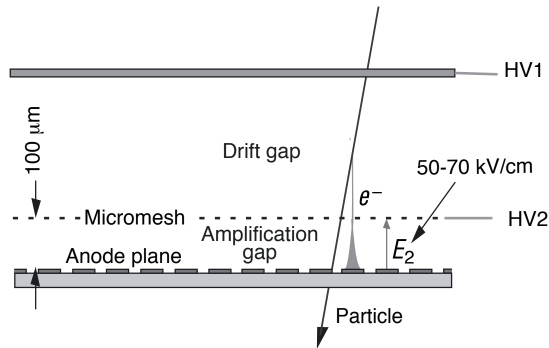

Figure 1.8 – *Operational principle of a Micromegas detector [50]. A particle crosses the detector and generates free electrons in the drift gap above the mesh, these electrons drift towards the holes in the mesh. In the amplification gap (below the mesh) the charge signal is amplified, it eventually reaches the anode readout plane.*

Micro patterned detectors

Micro-Pattern Gaseous Detectors (MPGDs) are detectors with micrometer size features, typically they are fabricated using microtechnology steps such as lithography. GEM and Micromegas are the most often used MPGDs. One of the earliest is the Microstrip Gas Counter (MSGC), originally developed by Oed [51], which uses micro-patterned anode planes for charge multiplication. Another MPGD that uses micro-technology fabrication steps is the μ-PIC introduced in [52].

The GEM and Micromegas detector lend themselves for an electronic readout array for imaging applications. Bellazzini *et al.* have coupled GEM detectors to dedicated CMOS imaging chips for high resolution imaging [53]. This detector has been used for UV photon imaging [54] and for x-ray astronomy [55]. Discrete, non-integrated Micromegas detectors have been coupled to Medipix imaging chips by Colas *et al.* [56] and the related work from the NIKHEF institute [57].

Several authors have presented hybrid detectors, consisting of various gaseous detectors. The total amplification is a result of the cascaded components. Capillary structures have also been used for this. These elements are similar to MCPs but have shorter aspect ratios, typically 1:10–1:30, they are normally referred to as Capillary Plates (CP). Examples are the combination of CP and MSGC by Tanimori *et al.* [58] and the hybrid detector presented by Peskov *et al.* [59]. Va'vra and Sumiyoshi [60] present a hybrid CP-Micromegas detector where the CP is used to limit the flow of ions created in the ionization multiplication. These ions can drift upwards (away from the readout plane) and damage the photocathode.

1.2 Experimental work on integrated photon detectors

The experimental work discussed in this thesis is focussed on two different types of detector, a gaseous detector and an MCP. Both are integrated, by post-processing, onto a CMOS imaging microchip for the readout of the created charge pulse. The two different concepts are outlined below. The detectors are made using microtechnology processing. Many of these techniques are known from IC processing or from MEMS processing. Because the detectors are built onto substrates with finished CMOS devices we speak of post-processing. It is essential that all post-processing is done in such a manner that the CMOS functionality is not compromised. The most important consequence of this is that during post-processing the substrates are not heated to temperatures higher than 450 °C. An overview of post-processing possibilities and requirements is given in [61].

1.2.1 Integrated Micromegas for photon detection

InGrid, which stands for Integrated Grid, is a detector with Micromegas layout that is integrated with a CMOS readout structure. In most cases we use the Medipix2 [62] or Timepix [63, 64] chips that are designed and fabricated in the CERN-led Medipix consortium [65]. The chips are discussed further in section 4.2. The thesis of A. Fornaini [66] is also of interest for its treatment of the Medipix chip.

The grid of the InGrid device is a thin Al layer (typically 1 μm). It is suspended from the anode plane (the imaging chip) by isolating pillars of 50–100 μm height. The pillars are made out of SU-8, a polymer photoresist material. The use of lithographic techniques to define the pillars means there is excellent control over the shape, size and placement of the pillars. The pillars are placed at the intersection of pixels so that they do not block any signals. The holes in the grid are also aligned to the pixel structure.

The first such detectors have been explored by M. Chefdeville and V.M. Blanco Carballo and co-workers. Good references are their theses [37, 67] and publications such as [68, 69]. These detectors where initially used for the imaging of ionizing radiation by detection of single, individual free electrons, both for 2D imaging as well as for 3D reconstruction using a Time Projection Chamber (TPC) [37].

This thesis documents the first use of these detectors for photon detection. To make the detectors photon sensitive a CsI photocathode is deposited onto the metal grid. Details on the process used to manufacture the InGrid device and the photocathode are given in chapter 4. Experimental results are presented in chapter 5.

1.2.2 Integrated MCP for photon detection

Another integrated photodetector is made using an MCP structure. An integrated MCP structure is built directly onto an anode readout plane (the imaging chip), on top of the MCP a photocathode is deposited. The photocathode might partially deposit on the sidewalls of the holes, down to a depth comparable to the pore width. The integration of the photocathode onto the top surface might limit detection efficiency due to the low photocathode surface area. In that case the photocathode might have to be placed on a separate window mounted above the detector. We have not focused on these issues related to the integration of the photocathode. Instead the experimental work is targeted on methods to fabricate a porous structure with IC compatible methods. The required pore geometry is determined, several fabrication techniques are proposed and tested. This is documented in chapter 6.

1.3 SU-8 as a construction material

In both devices discussed in section 1.2, SU-8 is a construction material that is considered. SU-8 is a negative tone photoresist [70] that was originally developed by IBM Research. It is widely used in microtechnology. SU-8 can be spin cast with thicknesses covering a broad range from 1 μm to 1 mm. For this a series of products differing in viscosity is available [71]. These layers can be patterned using standard UV lithography techniques, for instance using mask-aligners for contact lithography. Very high aspect ratio structures can be made, both for dark-field and light-field structures (although light-field structures are more difficult to develop).

The material is based on the EPON SU-8 monomer from Shell Chemical. Each SU-8 monomer has eight epoxy sidegroups, hence the 8 in its name. SU-8 is a negative tone photoresist meaning that it crosslinks under illumination. Because of the high number of epoxy bridges that can be formed the crosslinked material is very strong.

Initially SU-8 was intended for use as a sacrificial photoresist mask, for instance for molding processes. These applications are well matched to the strengths of SU-8 mentioned above; they do however require that the SU-8 can be removed. This has proven to be one of the main bottlenecks in using SU-8. Because the material is very hard and stable, it is difficult to remove it successfully [72, 73]. Successful stripping can for instance be achieved with (long) O_2 plasma ashing or Piranha cleaning. Both of these can have detrimental effects on, for instance, many different metal layers. As a result other types of resists have been formulated for sacrificial applications, for instance KMPR [74]. There have been efforts on using SU-8 in combination with a dedicated release layer, [75] shows a nice application of this technique, also many alternative release layers are referenced.

This technique is complicated; successful stripping is not guaranteed because the release step is very geometry dependent and the released structures can break upon release if they are too brittle.

The material's robustness to further processing has inspired researchers to employ SU-8 for permanent structures. The majority of reported applications currently use SU-8 as a structural material. The cross-linked material is an integral part of the device that is not removed in later processing. The material has been used to make micro-fluidic devices, cantilevers, optical devices and many other structures. Many examples are referenced in an excellent review publication [76] on SU-8 focusing on lithographic patterning capabilities.

1.3.1 Standard SU-8 process

Like most photoresists SU-8 contains three main components. The first component is the SU-8 polymer itself; it is highly cross-linkable in an acidic environment. Next is a salt-based Photo Acid Generator (PAG). The last component is a solvent. The results in this thesis have all been obtained with the original Microchem SU-8 formulation which uses gamma-butyrolactone (GBL) as a solvent. There are currently two other SU-8 types available as well, with different solvents. SU-8 2000 provides improved coating and allows faster soft-bakes, SU-8 3000 is a version with improved adhesion to many materials, especially to glass substrates. In chapter 6 some structures are made with conventional SU-8 in combination with solid SU-8 foil material. The foils were made available as an experimental product by Microchem, more details can be found in section 6.3.

The standard SU-8 processing that we use is described below; it is largely based on the recommendations given by the manufacturer (these can be found in [71]). If, for specific experiments, we have made alterations to the default process these are documented in the respective chapter. SU-8 is spun on using a conventional spin coater with spin speeds in the range 1000–3000 rpm. After spinning the layer is soft baked on a hotplate. The temperature is ramped up and down very slowly, from room temperature (RT) to 95 °C, to prevent cracking of the layers [77]. Usually conventional UV contact lithography is used to pattern the SU-8. SU-8 is a negative tone Photo-Resist. In the illuminated regions an acid will be generated by the PAG and this acid initializes the cross-linking of the polymer material. After the exposure a Post-Exposure Bake (PEB) is performed to accelerate the cross-linking reaction and to improve the contrast of the image. For the PEB it is also important to prevent temperature shocks, the heating is slowly increased from RT to 80 °C and then lowered back to RT after the required bake time. Normally the layers are then developed in a solvent, most often this is acetone or the dedicated SU-8 developer PGMEA. After the development the wafers are rinsed with isopropyl alcohol (IPA). Aqueous solutions are not used as water

may seep into the layers and deteriorate the layer quality and performance. After development a final Hard-Bake (HB) step may be given to strengthen the layer, remove small cracks and improve adhesion [78, 79]. This is normally done on a hotplate at temperatures between 120 and 180 °C [71]. A further discussion on HB steps is given in section 2.3.4.

1.3.2 SU-8 characterization

Many aspects of the SU-8 material and its application are part of or referenced in the review publication [76]. The mechanical aspects have been studied widely [80, 81, 82, 83]. Some of these studies pay special attention to the behavior of SU-8 during bakes and the effect of bakes on its mechanical properties [84, 85]. Other studies have been performed on the radiation hardness of SU-8 [86], which is interesting for sensor and space applications.

Dielectric behavior of SU-8

When SU-8 is used for high-voltage applications it is important to know the dielectric aspects of SU-8; this includes the relative dielectric constant and the dielectric strength. This last metric we consider to be the maximum electric field that a layer of SU-8 can sustain before the onset of excessive leakage current and/or electric breakdown. There are some statements given in the datasheets presented in [71], but the presented data is far from complete and information regarding measurement methods is also lacking. Thorpe *et al.* have, in [87], presented measurement data on the use of SU-8 as a dielectric for microwave structures and a characterization of the high-frequency loss factor of the material. They report that SU-8 has a relative dielectric constant of ca. 4.

Because of the lack of experimental data regarding dielectric strength we have performed an investigation, the results of which are presented in chapter 2.

Outgassing from SU-8

Similar to the situation regarding electrical properties, there are not many studies published on the outgassing behavior of SU-8. Two noteworthy exceptions are reports on effects attributed to remaining solvents [88, 89]. It was necessary to gather more information tailored for the use of SU-8 in ambients with a critical gas composition or in vacuum. We have studied the outgassing of fully processed SU-8 layers as they would be used in final products. This experimental work is presented in chapter 3.

SU-8 used in integrated photon detectors

We established that SU-8 has a remarkably high dielectric strength (chapter 2) and exhibits acceptable outgassing (chapter 3). This makes it suitable for use in the integrated photon detectors presented in chapters 4 to 6.

Chapter 2

Dielectric strength of SU-8

2.1 SU-8 in High-Voltage applications

We have investigated the Dielectric Strength (DS) of SU-8 in order to find the limits of the material for high voltage (HV) applications. We reported our first findings in [90]. New, more detailed results with data from improved test structures that allowed to quantify the dielectric strength were presented in [91]. The DS of SU-8 has not been documented yet in scientific literature. Some statements can be found on websites. For instance, on the datasheet that can be found in [71] of the special purpose SU-8 2000 and 3000 products the dielectric strength is specified as 1.1–1.2 MV/cm, but measurement conditions or other details are omitted.

We define the dielectric strength as the maximum electric field (E_{BD}) that can be applied before immediate breakdown for a given thickness. For well-designed test structures (with effective edge-termination) the dielectric strength approaches the one-dimensional critical field strength of the material. Generally, for long term stability, a system should operate at fields well below the dielectric strength of the materials used.

In the previous chapter we have seen two types of electron multipliers that can be used for photon detection. One type is the gaseous detector, such as the integrated Micromegas-type grid structure (InGrid) or other gaseous detectors such as the Gaseous Electron Multiplier (GEM). The other type is an integrated Micro-Channel Plate (MCP) structure that operates in vacuum. In both types (gaseous and vacuum) multiplication occurs through a controlled avalanche process sustained by a high electric field. For both types of devices dielectric layers are needed that can handle the voltages required to create the high electric field. SU-8 can be considered for both types of structures. Typical bias voltages for integrated gaseous detectors are 400–500 V for structures of 40–80 μm high. This means the maxi-

mum electric field is not more than 12 V/μm. In vacuum multipliers the requirements are higher, these are typically biased at up to 100 V/μm. These detectors are often made of quartz glass which has a dielectric strength of ca. 800 V/μm.

2.2 Experimental details

Many applications use SU-8 layers with a thickness of several tens of micrometers. It is very difficult to directly test the dielectric strength of such thick layers because the extremely high test voltages require exotic equipment and safety precautions. Besides, the edge termination (to avoid early breakdown at the edges) of test structures becomes much harder to make. For these reasons we have carried out breakdown tests only on thinner structures, with SU-8 thickness in the range of 2 to 15 μm. Breakdown voltages are then well below 10 kV. These layers are made of SU-8 2 and SU-8 5, which are different formulations of the same material, differing only in the fraction of solvent. The final epoxy matrix is the same and we therefore expect that the results obtained are of general relevance to other SU-8 layers.

2.2.1 Electrical test structures

The test structures used for dielectric strength evaluation are Metal-Insulator-Metal (MIM) capacitors with a mesa structure. Figure 2.1 shows such a device with a concentric circular layout. The overlap of the bottom electrode over the dielectric is always 0.2 mm on all sides. The overlap of SU-8 over the top electrode is varied from 0.05 mm to 0.2 mm and in another set of devices from 0.2 mm to 5 mm. These large overlap values are intended to keep the surface leakage current negligible. The lateral size of the devices is in the mm regime. The size s of the top electrode varies from 0.1 mm to 5 mm. The abnormally large surface area of the devices is needed to obtain measurable results with our test equipment, both in terms of leakage current and capacitance, when the dielectric thickness is increased to tens of micrometers.

2.2.2 Processing of test structures

The test structures presented in this paper are made in a manner similar to that for the InGrid structures (see chapter 4). The process is illustrated in fig. 2.2 and is described in more detail below. The SU-8 processing follows the guidelines from the vendor [71], unless specified otherwise.

First the metal bottom electrode is made by sputtering 1 μm of Al on top of a substrate. The devices are made on top of a carrier Si substrate with a thermally grown oxide layer of ca. 900 nm. The Al is patterned using lithography,

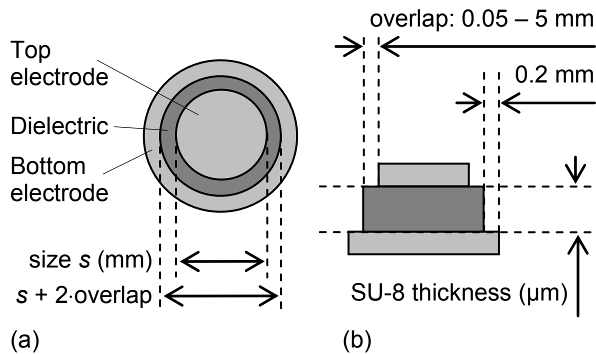

Figure 2.1 *– Illustration of an SU-8 capacitor test structure, top view (a) and cross-section (b). The most important design parameters are the size and the SU-8 overlap which determines the degree of isolation.*

PAN etchant (Phosphoric-Acetic-Nitric acid [92, p. 534]) at 55 °C and resist strip (10 min fuming HNO_3), see fig. 2.2a.

SU-8 is spun on using a conventional spin coater with spin speeds in the range 1000–3000 rpm. The processing conditions are given in table 2.1. After spinning the layer is first left to settle for 40–60 minutes on a hotplate set to room temperature (RT); this reduces the edge-bead [1]. Then the temperature of the hotplate is increased, for a soft bake at 95 °C. Conventional UV contact lithography is used to pattern the SU-8. After the exposure a Post-Exposure Bake (PEB) is performed to accelerate the cross-linking reaction and to improve the contrast of the image. These steps are the standard SU-8 process described in section 1.3.1, the resulting structure is depicted in fig. 2.2b.

In standard SU-8 processing the resist image is now developed in acetone or the standard SU-8 developer PGMEA. For the MIM capacitor structures the development step is delayed until the top electrode is formed. The uncross-linked SU-8 is used as a sacrificial material for support of the top aluminum layer. This is the most straightforward method to reliably define mesa structures of this type. On top of the SU-8 layer a 500 nm thick Al electrode layer is deposited by low power sputtering. This metal layer is patterned using lithography and wet etching, fig. 2.2c. The resist is cured at low temperature (30 °C) and the wet etch is performed at room temperature for an extended period.

Finally the SU-8 layer is developed. By design all un-exposed, un-cross-linked

[1]Spin casting results in a homogenous thickness due to the balance between centrifugal force and surface tension. At the edge of the substrate this balance is distorted creating a thicker ring of material, this is known as an edge-bead

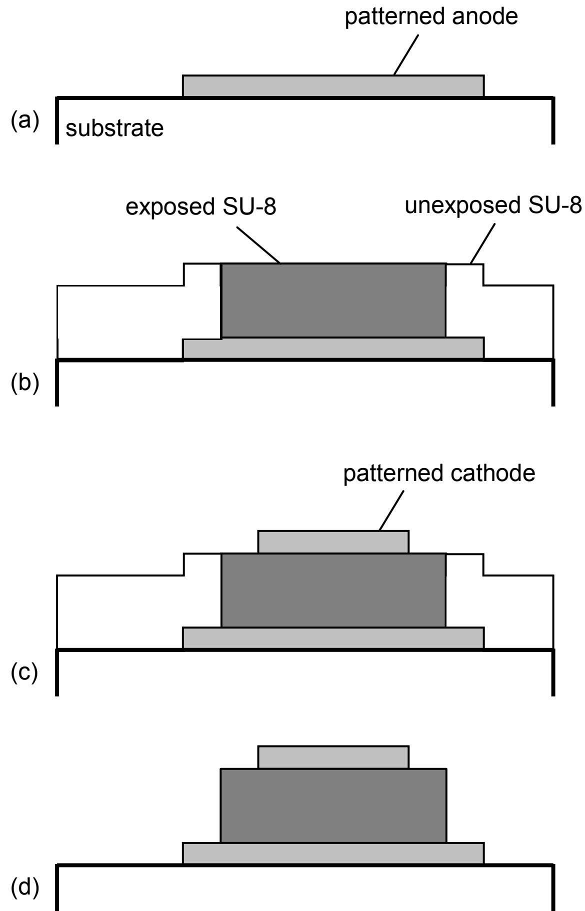

Figure 2.2 – *Overview of the processing sequence followed to make the test structures. The layer thickness of SU-8 was varied by using the spin conditions given in table 2.1. Two different dilutions of SU-8 have been used to reach the required thicknesses. The different layers also require adjustments to the baking times and the exposure dose. The thickest layer has been made by repeating the coat and soft-bake step.*

Table 2.1 – Process conditions used to fabricate different SU-8 layers

Material type	Spin speed	Soft-Bake time	Exposure dose	PEB time	Measured thickness
-	[rpm]	[min]	[mJ/cm^2]	[min]	[μm]
SU-8 2	2000	4	140	4	2.16–2.25
SU-8 2	1500	4	140	4	2.74–2.85
SU-8 2	1000	4	140	4	3.88–3.93
SU-8 5	3000	4	140	4	4.97–5.09
SU-8 5	2000	7	180	5	7.1
SU-8 5	1000	7	180	5	13.1
2 × SU-8 5	2000	2 × 7	240	5	19.0

regions are directly exposed to the developer. Development is done by immersion in acetone at room temperature using ultrasonic excitation. The development progress is checked visually. Development takes between 5 and 10 minutes depending on the layer thickness. The final result is shown in fig. 2.2d.

The deposition parameters have been optimized for mesa structures; they are different from the settings used for the InGrid structures with a suspended metal grid (chapter 4). Despite the optimization it is still possible that a skin of cross-linked SU-8 forms at the top of the unexposed sections of the resist layer. Long development times and ultrasonic excitation are needed to remove these thin skins of (partially) cross-linked material. An additional cleanup step is performed in Microstrip 5010 ($\sim$30 min, at room temperature) to remove residues.

The final thickness after processing has been measured using a Dektak profiler, the results are presented in table 2.1. Each thickness given in the table is an average over 5–10 measurements. The experiments on the first four, thinner layers have been repeated several times, the thickness range given is the range found among the averages for all wafers.

2.2.3 Electrical characterization

High voltage current-voltage (HV-IV) measurements are performed on a Karl Süss PM8 probe-station using a purpose-built probe with a non-conductive arm. We measured I-V characteristics by applying a bias voltage using a Fug HCN 200 K 12500 source and measuring the current with the Source Measurement Unit (SMU) of an HP 4156B Parameter Analyzer. The measurement set-up is shown in fig. 2.3.

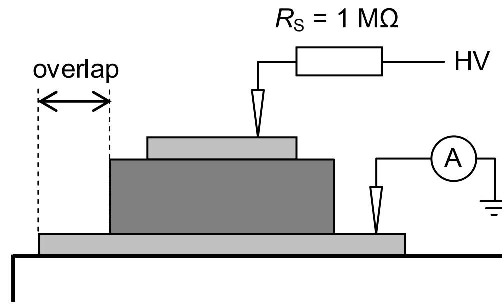

Figure 2.3 *– Measurement set-up showing the device connected to the SMU of an HP 4156B parameter analyzer used as a current-meter and the high voltage bias connected in series with a high-ohmic protection resistor.*

To prevent discharges a special, dedicated, probe has been made. In a normal probe the coaxial (or triaxial) orientation of the signal and ground and shield leads is maintained to very close to the probed surface in order to limit aberrations due to capacitive/inductive coupling. With our HV probe however the shield ends some distance (several cm) before the probe needle to prevent discharges. The probe arm is made out of Teflon (instead of metal). The mechanical manipulator is that of a standard Karl Süss probe. Figure 2.4 shows the purpose built probe. The cables are interconnected using Radiall SHV connectors. All measurements were done under dry N_2 atmosphere. To prevent deformation of the SU-8 layer by the probing needle the contact has to be made relatively gently. Probing is always aimed at the centre of the top electrode. Reproducible leakage currents are obtained in a large range of needle pressures. Until breakdown no material deterioration of the probe location is observed, in the event of breakdown through the dielectric the destruction of the layer starts at the probe location.

The other terminal of the device is contacted with a standard SMU of an HP 4156B parameter analyzer. This terminal is kept at 0 V and the current is sampled continuously using a long integration time. Typically it takes 2–5 s for the current to stabilize. To limit the dielectric breakdown discharge current as well as to shield the current sensing SMU from the high voltage, a protection resistor is connected in series with the device at the high side. For the presented measurements we have used a resistor network with an effective 0.99 MΩ series resistance and a maximum power rating of 8 W. Additional measurements have been performed on thicker layers (7 to 19 μm). These measurements are made using a simpler set-up. Precise measurement of the current is not possible but higher voltages can be reached. The bottom electrode is grounded, the high voltage is applied using a Danbridge JP 30-A high voltage source.

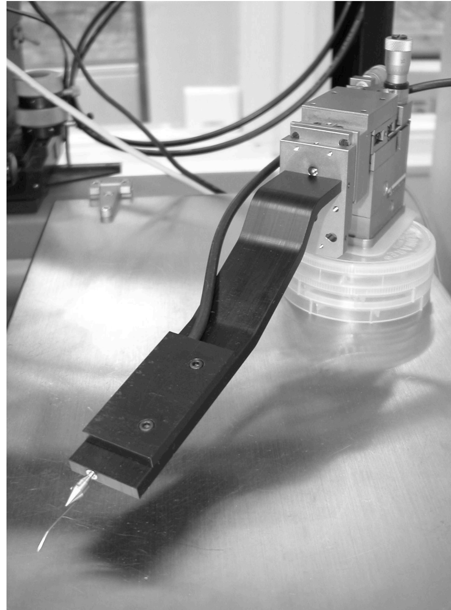

***Figure 2.4** – HV probe made by replacing the metal arm (optimized for coaxial shielding) with a Teflon arm optimized for isolation width.*

2.3 Results and discussion

2.3.1 Low-field conduction

We have measured bottom electrode current as a function of (positive) bias voltage applied to the top electrode. The bias was increased in steps of 50 V. Each time the current level is recorded after it has stabilized. The current increases steadily with voltage. Figure 2.5 shows curves of current density versus bias voltage, so called J-V curves. The figure shows the average and the 1σ spread obtained from a series of 9 devices on 4 different wafers with a varying SU-8 layer thickness. The current density is calculated by dividing the current with the top electrode area as measured after processing. We assume the current mainly consists of a bulk component that scales with electrode area and a surface (overlap) component that scales with the perimeter. From the initial results we conclude that well before breakdown ($V < 1000$ V) the area component is dominant.

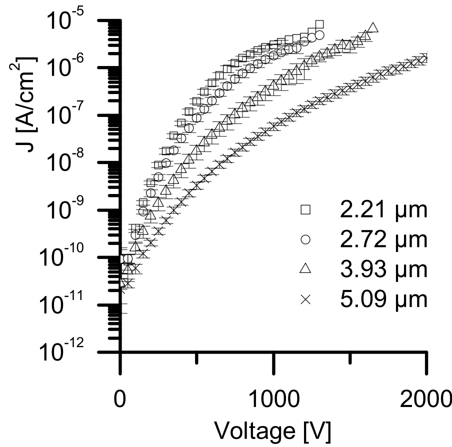

Figure 2.5 *– JV characteristics (average and 1σ spread) of different MIM-capacitors with a varying SU-8 thickness as stated in the legend. The current decreases with increasing thickness.*

2.3.2 Conduction mechanism

Conduction through the structure is influenced by two components: the conduction through the dielectric itself and the injection of carriers into the structure from the electrodes. By careful observation of the leakage currents we have determined which mechanism is the limiting factor. The J-V characteristics presented in fig. 2.5 show that the behavior is strongly non-ohmic, suggesting that the transport is dictated by injection from the dielectric-metal interface. In fact if current density is plotted against electric field strength E (shown later) we see that the curves for devices with different thickness fall on top of each other over almost the entire range. This proves that the conduction is not limited by resistance in the layer which must scale with thickness.

Electric field strength E is defined in eq. (2.1) in V/cm, where V is the bias voltage in V and t is the thickness of the SU-8 layer in cm.

$$E = V/t \tag{2.1}$$

Because the electric field strength is not very high we assume that Fowler-Nordheim injection is limited [93, p. 228], and that thermionic emission is dominant. Thermionic emission [93, pp. 157, 227, 228] can be described by the formula given in eq. (2.2). Here J is current density in A·cm^{-2} , A is the Richardson constant in A·cm^{-2}·K^{-2}, T is absolute temperature in K, W is the energy of the charge carriers in eV, and k is the Boltzmann constant ($8.620 \cdot 10^5$ eV/K).

$$J = A \cdot T^2 \cdot \exp(-W/kT) \tag{2.2}$$

The carrier energy W is determined, as shown in eq. (2.3), by φ_{Al} the work function of Al (4.28 eV), $\chi_{\text{SU-8}}$ the electron affinity of the dielectric SU-8, and ΔW, a barrier lowering due to the applied bias.

$$W = \varphi_{\text{Al}} - \chi_{\text{SU-8}} - \Delta W \tag{2.3}$$

The shift ΔW due to the bias field strength is defined in eq. (2.4), where e is the elementary charge ($1.602 \cdot 10^{-19}$ C), E is the electric field strength, ϵ_{rel} is the relative permittivity of the dielectric ($\sim$ 4), and ϵ_0 is the absolute vacuum permittivity ($8.854 \cdot 10^{-14}$ F/cm).

$$\Delta W = \left(\frac{e \cdot E}{4\pi \cdot \epsilon_{\text{rel}} \cdot \epsilon_0} \right)^{1/2} \tag{2.4}$$

Combining eqs. (2.2)–(2.4) we reach the following eq. (2.5) for the logarithm of current density $\log(J)$.

$$\begin{aligned} \log(J) &= C + \Theta \cdot \sqrt{E} \\ C &= \log\left(A \cdot T^2 \cdot \exp\left(\frac{-(\varphi_{\text{Al}} - \chi_{\text{SU-8}}}{kT} \right) \right) \\ \Theta &= \left(\frac{e}{4\pi \cdot \epsilon_{\text{rel}} \cdot \epsilon_0} \right)^{1/2} \cdot \frac{1}{kT} \end{aligned} \tag{2.5}$$

In fig. 2.6 the leakage current through the SU-8 layer is plotted logarithmically against the square root of the electric field across the dielectric. This is done for 4 different SU-8 layer thicknesses. As can be seen in the plot the leakage current scales logarithmically with the square root of electric field in a wide current range.

The leakage current level is determined by the electric field strength at the interface where the current is injected; it does not depend on SU-8 layer thickness as can be seen by the nearly identical curves obtained for the different layers. Only the wafer with the thickest SU-8 layer (5.09 μm) has slightly lower current. This cannot be explained by measurement errors in the bias voltage or the thickness of the layer. It is noted however that the three thinner layers are made with SU-8 2 whereas the thickest layer is made with the more viscous SU-8 5 product.

The leakage current density is strongly temperature dependent. Equation eq. (2.2) is reformulated as eq. (2.6).

$$\frac{J}{T^2} = A \cdot \exp\left(\frac{-(\varphi - \Delta\varphi)}{kT} \right) \tag{2.6}$$

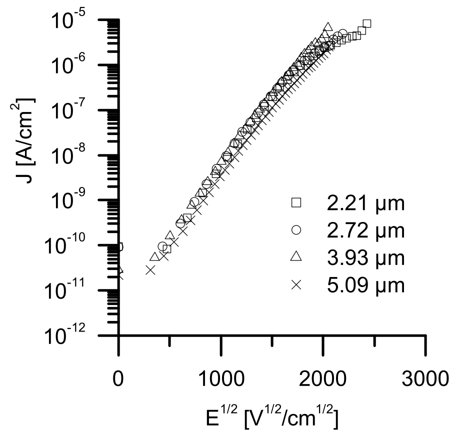

Figure 2.6 – *Leakage current density vs. the square root of electric field strength for devices with different SU-8 thicknesses.*

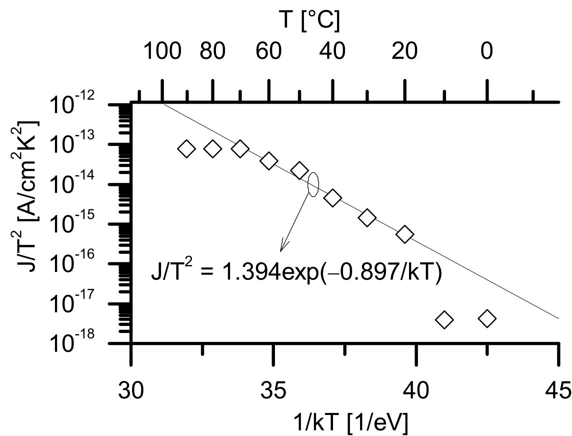

Figure 2.7 – *Plot of J/T^2 vs. $1/kT$, leakage current density is measured at a bias voltage of 200 V. The temperature was varied from 0 to 90 °C.*

Figure 2.7 shows J/T^2 plotted against the inverse of thermal energy kT (in units of 1/eV). We see that for the temperature range from room temperature until 80 °C (which is just below the highest temperature reached during processing of the structure) the metric $\log(J/T^2)$ scales with the inverse of temperature.

The linear behavior seen in the two graphs presented points out that the leak-

age current is determined by thermionic emission of carriers from the Al electrodes into the dielectric material. Using a logarithmic fit made to the data presented in fig. 2.7 the coefficients A and energy W $(= \varphi - \chi - \Delta W)$ can be determined. We obtain a value of $A = 1.394\ \mathrm{A \cdot cm^{-2} \cdot K^{-2}}$. The Richardson constant is a physical parameter which is linearly proportional with the effective mass of the electron. In vacuum, where $m_e = m_0$, the value of A is $120.2\ \mathrm{A \cdot cm^{-2} \cdot K^{-2}}$. Our measurement suggests therefore that the effective mass of electrons in SU-8 is around $0.012 \cdot m_0$. The carrier energy is $W = 0.9$ eV. At a bias level $V = 200$ V the shift ΔW is found to be only 0.12 eV. The difference in work function from the metal to the dielectric is therefore $0.9 + 0.12 = 1.02$ eV. The work function of Al is 4.28 eV [9, p. 137]. We find an electron affinity of 3.24 eV for SU-8.

2.3.3 Dielectric strength

When the bias is increased, breakdown occurs, at which point the current rapidly increases and saturates. The breakdown causes irreversible damage to the device. We have seen cases where breakdown occurs in the middle of the device, through the dielectric. Figure 2.8 shows the device before and after such breakdown events in part a) and b). Also, in some cases, we have seen breakdown laterally across the isolation width from the side of the top electrode to the nearest point of the other electrode. Current flows across the surface of the SU-8, which does not usually lead to an immediate short. If the high current is sustained for some time a very large part of the top electrode will be consumed, as shown in fig. 2.8c.

Some device designs have a shorter isolation width. The device in fig. 2.8d has an isolation width of only 0.2 mm. The entire device, top electrode, SU-8 overlap and bottom electrode can be seen. In these devices breakdown is almost exclusively edge-breakdown and it usually results in a rapid creation of a black deposit across the isolation overlap that effectively shorts the two electrodes, this can be seen in fig. 2.8e.

The Breakdown Voltage (V_{BD}) is defined as the highest voltage that can be applied before the current rises uncontrollably. The current is always ramped up slowly.

Figure 2.9 shows V_{BD} (average and 1σ spread) measured on devices with varying dielectric thickness. The first four points (diamonds) were measured on the same devices as used for the leakage current measurements. The open squares represent additional data points with larger SU-8 thickness. These are measured with a simpler set-up (as outlined in section 2.2.3). With a linear fit through all data points we determine that the dielectric strength of SU-8 is $443 \pm 16\ \mathrm{V}/\mu\mathrm{m}$ or 4.43 ± 0.16 MV/cm (1σ) for SU-8. This value is independent of whether or not an additional hard-bake of the SU-8 is performed; this is experimentally verified for a hard-bake of 20 min at a temperature of 150 °C, see section 2.3.4.

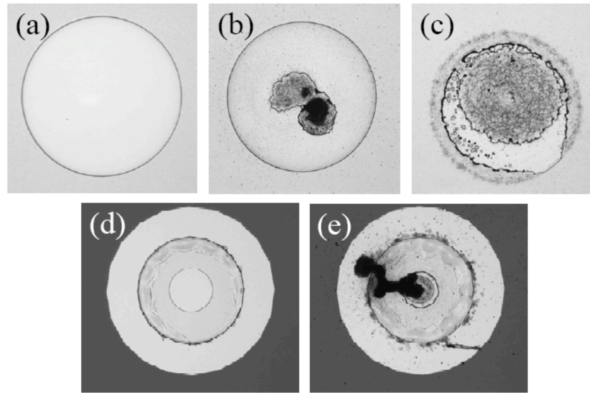

Figure 2.8 *– Top electrode area of devices, a) before breakdown measurement, b) after centre (bulk) breakdown, c) prolonged edge breakdown, d) device with small isolation width before breakdown and e) after edge breakdown.*

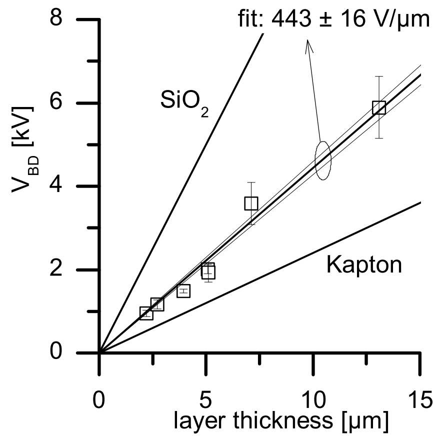

Figure 2.9 *–* V_{BD} *of SU-8 plotted vs. thickness, the dielectric strength of SU-8 and of two other materials is indicated with drawn lines.*

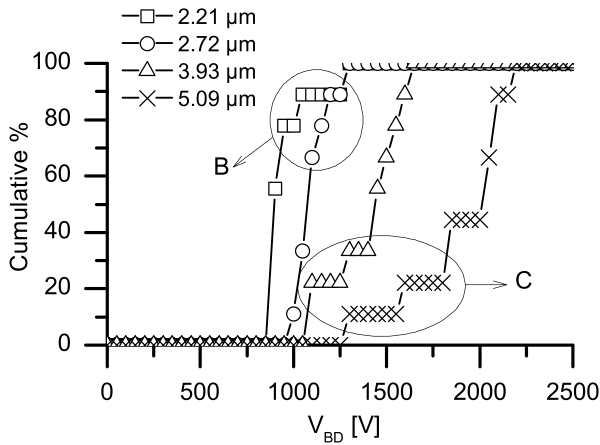

Figure 2.10 *– Probability plot showing different Break-Down modes: intrinsic BD in the middle (B) and pre-mature BD on the edge (C) of the device.*

For reference the dielectric strength of two other materials is also indicated in Figure 2.9. The dielectric strength of SU-8 (4.4 MV/cm) is higher than that of Kapton (2.4 MV/cm, CR or HN variety) [94, 95], as well as that of other similar construction materials such as Parylene N (2.8 MV/cm) [96] and PEEK (0.2 MV/cm) [97]. Kapton is a polyimide material that is very often used for gaseous detectors such as GEM foils (introduced in section 1.1.3). For gaseous detectors (see section 1.1.3) in general the DS is required to be > 1 MV/cm. The performance of SU-8 exceeds this requirement easily. The value we obtain is also significantly higher than the value of 1.1–1.2 MV/cm specified in the datasheet for SU-8 2000 and 3000 [71].

The dielectric strength of thermally grown silicon-oxide (SiO_2, 8–9 MV/cm for thick layers) is also indicated in the graph. The dielectric strength of SiO_2 is one of the highest achievable and it certainly has the highest dielectric strength found among materials used in conventional micro-electronics. The dielectric strength of SU-8 reaches as much as 50% of that of SiO_2.

Figure 2.10 shows a cumulative histogram of the breakdown distribution for various layers. For the thinner layers the breakdown occurs almost exclusively in the centre of the device (situation B, shown in fig. 2.8b). We consider this the intrinsic breakdown of the dielectric material. For the thicker layers the breakdown voltage becomes so high that we more often observe a preliminary breakdown at the perimeter of the device (situation C). This results in a severe erosion of the top electrode as illustrated in the micrograph in fig. 2.8c.

From this and other results above we conclude that edge-termination of HV

biased SU-8 structures is critical. A large enough overlap is required to prevent destructive discharges along the surface. The devices in fig. 2.10 have an overlap distance from 0.2 mm to 5 mm. The thinnest devices show intrinsic (bulk) breakdown around 1 kV. For these devices the smallest overlap of 0.2 mm is sufficient to prevent early (surface) breakdown. For the thicker devices we see a larger variation in breakdown voltage and corresponding mode. These devices require a larger isolation width to consistently observe intrinsic bulk breakdown. From 2 mm onwards breakdown values become stable. We have performed our measurements in an N_2 ambient. Surface breakdown will be strongly suppressed in the Ne, Ar or He based gas mixtures typically used in the gaseous radiation detectors [36]. Specifically the additional molecular gas fraction that is added to these mixtures, such as CH_4, isobutane or DME, increase the breakdown strength greatly. Therefore we have not investigated surface breakdown effects further.

2.3.4 Influence of Hard-Bake steps on the dielectric strength of SU-8

If SU-8 is processed correctly, especially the PEB needs to be sufficient, the polymerization level is very high. Each SU-8 monomer has 8 epoxy bridges and a large fraction of these will be made. The structure is hard and has many advantageous mechanical properties. Despite this SU-8 layers are occasionally given a Hard-Bake (HB) step to alter the properties of the layer. With a HB the polymerization can be increased even more, as is suggested in the guidelines provided by the manufacturer [71]. A HB step is normally performed on a hot-plate, in air, for a period of 20–30 min. Typical temperatures are 120–150 °C. The HB is often done directly after development of the SU-8 structure but it can also be delayed until later in the process.

HB steps are not without debate, apart from the polymerization level there are many more effects, some may not be beneficial. In all cases it is important to experimentally verify the effect of including a HB step on the entire structure. Some reports claim that HBs promote cracks [98] others claim that they provide stress relief and can overcome problems with cracks and adhesion [78]. Recent findings on SU-8 adhesion properties indicate that Hard-Bake steps can have a strong positive effect on adhesion strength [67].

We have tested the effect of HB steps on the electrical properties of SU-8 layers. This is an extension of the previous experiments. The methods are completely identical except that some structures have been given an additional hotplate HB process at 150 °C for 20 min. We have measured the thickness of the SU-8 layers before and after the HB, there was no significant difference.

The Dielectric Strength is measured in the same manner as before on samples with and without Hard-Bake. Figure 2.11 shows the dielectric strength of samples

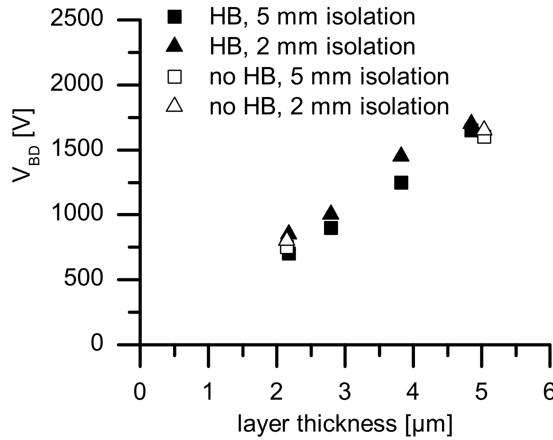

Figure 2.11 *– Dielectric strength of different SU-8 layers with and without Hard-Bake. There are two sets for two different isolation widths (2 and 5 mm), because for these conditions 2 mm is sufficient there is no difference between the two sets. Also the HB does not seem to influence the DS.*

with and without a Hard-Bake. The DS is not affected by the HB. Leakage levels, measured before breakdown, were also of the same order in both sets of devices. The DS in these devices is overall 371 ± 15 V/μm. This is 15% lower than the original value presented in section 2.3.3.

The capacitance of the test devices is measured with an HP 4282A *LCR*-meter. The bias voltage was 0 V and the excitation voltage was 100 mV. The relative permittivity of the devices is calculated from the measured capacitance. We assume the test devices behave as parallel plate capacitors. The device dimensions have been measured after fabrication. The results are presented in fig. 2.12 for two sets of devices, one with an SU-8 thickness of 2 μm and one of 5 μm. The results are similar for both thicknesses. The samples that have received a Hard-Bake show significantly lower (10–15 %) permittivity. One explanation for the capacitance decrease could be the loss of water or other volatile components in the dielectric layer due to the bake step. Another hypothesis is that the material characteristics at the interface change during the bake due to a reaction between SU-8 and Al. To explain the results the interface layer would need to have a low dielectric constant with respect to SU-8. We cannot rule this out based on the present information.

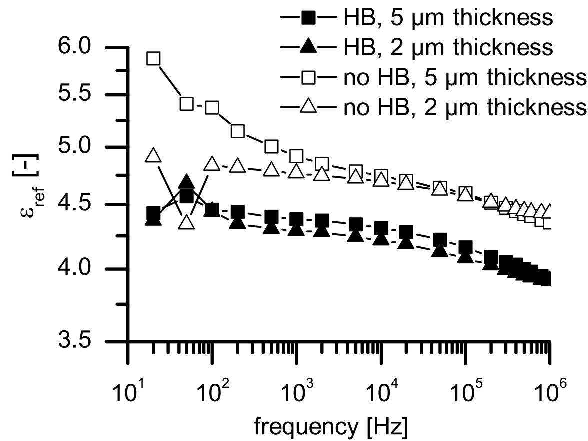

Figure 2.12 *– Relative permittivity of various SU-8 layers, with and without HB and of 2 and 5 µm thickness. For both thicknesses the permittivity of the layers drops after applying a HB.*

2.4 Conclusions

We have presented measurements on the dielectric behavior of SU-8 under low- and high-voltage bias conditions.

The leakage through SU-8 is found to be a reliable and repeatable smooth function of voltage and, at least for the very large device sizes used here, the current scales well with the contact area. The leakage current density through the dielectric layer scales logarithmically with the square root of bias field strength ($E^{1/2}$) and the logarithm of J/T^2 is inversely proportional with temperature. This indicates that thermionic emission from the Al electrode causes the leakage current. The electron affinity of SU-8 is determined through measurement, the value is 3.24 eV.

The dielectric strength of SU-8 is 4.43 ± 0.16 MV/cm. This value is remarkably high for a polymer material, it is more than sufficient for the requirements of gaseous radiation detectors. The DS is also high enough for the use of SU-8 in vacuum operated electron multipliers such as MCPs. The DS of SU-8 is not influenced by additional Hard-Bake steps. A suitable edge-termination is essential for SU-8 structures if they are subjected to high bias voltages. Due to the high intrinsic dielectric strength of the material a large overlap of the dielectric with respect to the electrode is needed.

Chapter 3

Outgassing from SU-8

We have so far considered SU-8 for the use in two different types of electron multiplying structures, (integrated) MPGDs (section 1.2.1) and capillary structures operated in vacuum (section 1.2.2). In both structures the composition of the ambient is very important for device operation. This means it is necessary to know the influence of the materials on the ambient. This is especially important if new materials are proposed, such as SU-8, that have not been used for these types of detectors before. It is important to know what is outgassing from SU-8 as well as how much is being released, i.e. at which rate. This work follows earlier work on the identification of outgassing species from detector building materials [99, 100]. These articles also deal with the effects of the material on detector aging. For the vacuum operated devices it is obvious that any gaseous material released from the detector will degrade performance. For MPGDs outgassing can also be important.

In gaseous multipliers the SU-8 is used to fabricate a structure that relies on a controlled avalanche process in a gas. The composition of the gas mixture is a very important parameter for the gain and the long term stability (or aging) of such a device. Typical gas mixtures have a large fraction of a noble gas, the high ionization probability results in a high gain. With only the noble gas however, the gain will not be controllable, the chamber is easily triggered into a continuous discharge. To prevent this a fraction of a molecular gas is added. These gases have much more non-ionizing modes of interaction, this quenches the behavior and allows stable operation at a high gain level. Gas molecules consisting of more atoms (the more the better) can absorb radiation through vibration and rotation around the bonds, this lowers photon feedback [36, p. 47]. Compounds that are outgassed by organic polymers such as SU-8 could very well influence the delicate balance of an optimized gas mixture.

Furthermore many aromatic compounds are found to have a strong effect on

aging. Initially it was conceived that benzene rings can be cracked by the plasma like environment created in the ionization cloud of an operating gaseous detector [99]. The radicals created in this manner lead to the deposition of polymers onto various detector surfaces. These deposits alter the device performance, this effect is known as aging. This hypothesis was disqualified by the absence of benzene dissociation products. Reference [100] instead suggests that it is not the aromatic compounds themselves but the addition of organic sidegroups from the quencher gas (or other sources) that lead to the creation of polymerizing species.

In this chapter we aim to make a qualitative and quantitative assessment of the outgassing from SU-8 layers. We use mass-spectrometry (MS) and Gas-Chromatography (GC) to find which compounds are emitted over time. These methods also allow to assess the outgassing rate expressed in terms of mass per time. Once the behavior of SU-8 is characterized we can use this information to optimize the processing, specifically the thermal budget. All thermal steps will influence the outgassing behavior, dedicated Hard-Bake steps can be included in the process to reduce the outgassing rate of the final product. Quantitative knowledge on the outgassing behavior of SU-8 is not only important for electron multipliers but also for many other applications. Example of this are the use of SU-8 for cantilevers that operate in vacuum or other hermetically sealed envelopes [101] and for the use of SU-8 in wafer-scale packaging [102].

3.1 Experimental methods

The SU-8 layers under study are formed on top of bare 4″ Si wafers. To prevent additional outgassing signals the wafers are first cleaned extensively in a bath of fuming (100%) HNO_3 at room temperature for 10 min followed by a rinse and another cleaning step in 69% HNO_3 at 95 °C for 10 min. Finally the wafers are rinsed again in DI water and dried using a spinner under flowing nitrogen. After this a short 2% HF dip is performed to remove native oxide, the hot 69% nitric acid step is repeated to re-grow a thin chemical oxide and the substrates are rinsed again. After a 10 min dehydration bake at 120 °C the SU-8 layer is deposited by spin coating at 3000 rpm; a primer is not used. The wafers are given a 20 min Soft-Bake at 95 °C, using a hotplate, to solidify the resist layer. Next a blanket UV exposure with a dose of 290 mJ/cm^2 is performed to initiate cross-linking of the entire layer. A Post-Exposure Bake is performed for 10 min at 80 °C. All bakes are done using long ramp-up and ramp-down times as per instructions given by the supplier [71]. The wafers are diced into 2 cm × 2 cm samples using a Disco DAD-321 wafer saw. Immediately after drying (using a N_2 spray gun) the samples are packaged in Al foil that is folded twice around the sample, the packaged samples are stored in sealed bags until they are measured. Some samples

have received an additional 10 min Hard-Bake (HB) at 150 °C, also on a hotplate, prior to packaging.

All initial measurements are performed on layers of SU-8 50 of 50 μm thickness. Additional measurements on thinner layers of 2 and 10 μm have also been performed. For these SU-8 formulations with a lower viscosity are used (SU-8 2 and SU-8 5 respectively), the spin speeds are lower and the bake times are shorter. Two analysis techniques have been used, Mass Spectrometry (MS) and MS combined with Gas Chromatography (GC-MS).

For MS analysis the SU-8 samples are placed in a vacuum chamber, a mass spectrometer (Pfeiffer QMS Prisma) is connected to monitor the gas flow coming out of the system. The specimen chamber can be elevated in temperature by resistive heating. In a first test we performed MS measurements to determine what species and compounds are being outgassed. At room temperature the outgassing rate of most materials is very low and the MS is unable to register anything. To allow detection the sample needs to be heated. We have heated the sample in the range of 150–200 °C. This is also the range that can be safely used for hard-bakes of SU-8 in dry air without damaging the layer [84, 103].

Further measurements are performed using a combined gas-chromatography and mass-spectrometry technique (GC-MS). This is the same analysis method used in [99, 100].

With GC-MS a much more detailed analysis can be performed than with MS only. It allows to determine the outgassing rate in quantitative terms, while simultaneously identifying which compounds are being released. The samples are heated in an oven that is flushed continuously with N_2. The outgassed components are adsorbed (except for the carrier gas) using a Gerstel TDSA tube and after a set period the sampled mass is released and injected into a gas-chromatography column (Agilent 5975) in which the exact chemical composition can be identified. This sampling is repeated over time to create a quantitative measure of outgassing rate and mass (accuracy is ∼5%). The technique is not sensitive for compounds with a mass lower than ∼40 a.m.u.

3.2 Results and discussion

3.2.1 Mass spectrometry measurements

Figure 3.1 shows a series of mass/charge spectra obtained from a sample that has received a 150 °C hard bake. For clarity only the part with $m/q > 30$ is shown. During the scans the temperature is increased to 200 °C and then allowed to cool down to room temperature again as indicated. At elevated temperature we see heavier compounds (in the range $m/q > 50$) being released (fig. 3.2). During the whole cycle m/q 44 is abundantly present. Although there is also a large

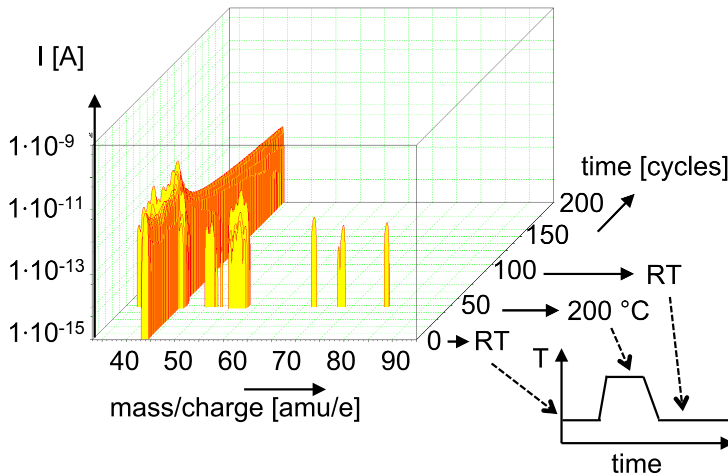

Figure 3.1 – *Outgassing measured, using a mass spectrometer, by continuous sampling of the mass range* $30 < m/q < 100$*, over time from a sample of SU-8 50. The sample is first heated from room temperature (RT) to 200 °C and then allowed to cool down. The whole mass range is continuously sampled, each spectrum takes app. 5 minutes. At the peak temperature we see a large amount of compounds being released. In addition, at all temperatures, we see a signal with* $m/q = 44$.

background signal for $m/q \sim 44$ (as can be seen after cooldown to room temperature) there is an increased contribution at elevated temperatures. The main candidates for this mass signal are CO_2 or propane (as suggested in [104]). An extended GC-MS measurement is performed to capture any possible propane contribution. This involves extra strong cooling to improve the collection efficiency of such very volatile gases. However, no traces of propane have been found in any of the samples. Although CO_2 cannot be measured using CG-MS the complete absence of propane suggests that during the measurement (at 150 °C) the material is decomposing and ultimately is released in the form of CO_2.

The mass spectrometry measurements show significant outgassing contributions of heavier compounds (in the range m/q = 50–200). After heat treatment the outgassing is limited. This provides a process window for the use of SU-8 in vacuum and/or hermetically sealed packages. If a Hard-Bake of at least 150 °C can be allowed the outgassing levels are comparable to Kapton foils of the same area as determined using the same measurement method [105]. Kapton is commonly used in other gas-filled detectors such as GEM foils.

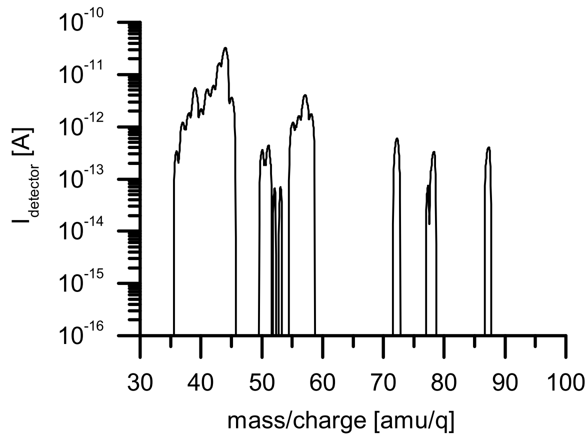

***Figure 3.2** – Typical outgassing spectrum of the material (50 μm SU-8) at the moment when T = 200 °C, this is when most material is released.*

3.2.2 GC-MS measurements

The GC-MS measurements indicate that most of the outgassing is constituted by butyrolactone (GBL, the solvent of the SU-8 resin), propylene carbonate (the solvent of the Photo-Acid-Generator (PAG)), benzene and di-phenyl-sulfide which is a component of the PAG. Examples of GC-MS spectra are shown in fig. 3.3. These show the outgassing at the start of the measurement series and at the end of the series (in this case after 80 minutes).

Using GC-MS we have determined the total outgassing rate in terms of weight loss over time. We have evaluated samples of SU-8 with a varying thickness of 1.7 μm, 9.2 μm and 50.9 μm SU-8. The thickness values are determined by step-height measurements using a Veeco Dektak 8 profilometer in combination with cross-section SEM inspections. The three different thicknesses are obtained by using three different SU-8 formulations. The thinnest layer is made with SU-8 2, the middle layer with SU-8 5 and the thickest sample was made with SU-8 50. The different SU-8 formulations only differ in the concentration of solvent that is added to the compound to change the viscosity and allow spin-casting with a different thickness regime. The procedures followed to make the different samples is similar to the one described in section 2.2.2 and the process conditions listed in table 2.1.

Figure 3.4 shows the total outgassing from samples of SU-8 with a different thickness. The plots show both the rate and the cumulative outgassed mass. In these linear plots we see that the rate starts high but after a short while (~10 min)

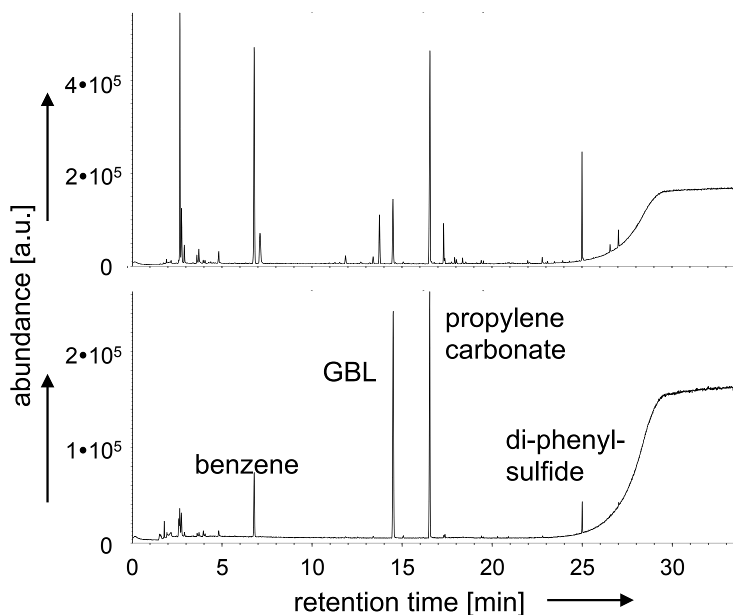

Figure 3.3 *– GC-MS spectra at the start of the measurement (top) and after 80 min (bottom), during the entire measurement period samples are taken, the SU-8 layers remain at high temperature (in this case 150 °C) the whole time. The results illustrate that after a certain thermal budget (comparable to a hard-bake) outgassing is limited to only several compounds, these compounds can be directly linked to the main components of SU-8. The spectra are plotted according to their retention time in the GC measurement, this is the time it takes for specific compounds to be released from the adsorption tubes into which samples of the analyte are adsorbed. Together with other data the time characteristic is used to identify the material.*

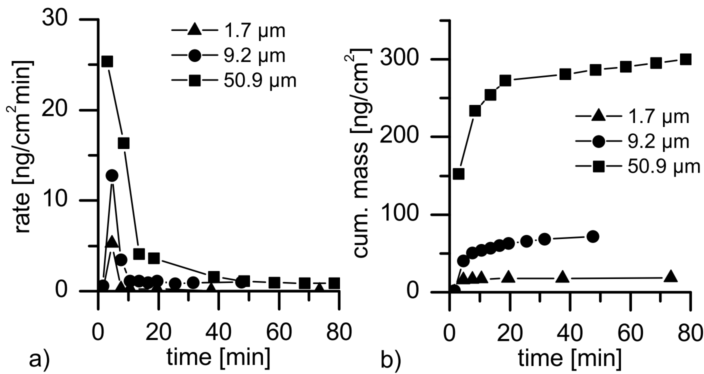

Figure 3.4 *– Outgassing rate as a function of time for three different SU-8 layer thicknesses as indicated, a) shows the total rate for each sample and b) the cumulative mass that has been emitted. The measurements were made using GC-MS, the data points represent the average outgassing rate over a sampling time of 3 min for the two thinnest layers and 5 min for the thickest sample.*

it drops significantly. Most of the outgassing is achieved in this first period.

Figure 3.5 shows the development over time of outgassing rates for various compounds as well as for the total from different SU-8 samples. This time the data is plotted on a log-log scale to allow more careful characterization of the process. To characterize the level of outgassing fits of the shape described in eq. (3.1) below are made to the measured time-resolved outgassing rates, q, where q_0 is a rate constant, t is time and α is a time constant.

$$q \propto q_0 \times t^{-\alpha} \tag{3.1}$$

The outgassing rate is characterized by the fit parameters α and q_0. The slopes (α) of the fitted outgassing rates are in most cases close to unity. This type of outgassing behavior, inversely proportional with time, is typical for many materials [106, ch. 4]. The constant q_0 is given in units of $\mathrm{ng} \cdot \mathrm{cm}^{-2} \cdot \mathrm{min}^{-1}$. For the thickest layer we find a total rate of $104\ \mathrm{ng} \cdot \mathrm{cm}^{-2} \cdot \mathrm{min}^{-1}$. This outgassing is mostly due to 2-propenal, a material with a molecular mass of 56 g/mol. Other constituents include benzene (with a higher molecular mass of 78 g/mol), and CO_2 (with a lower molecular mass of 44 g/mol). The last contribution can be deduced from the MS measurements presented earlier in this section (fig. 3.1 and accompanying text). If we assume the overall average molar mass to be that of the major component (2-propenal at 56 g/mol) we can convert the mass rate into a pressure-times-volume rate. This last metric is commonly used in literature [106].

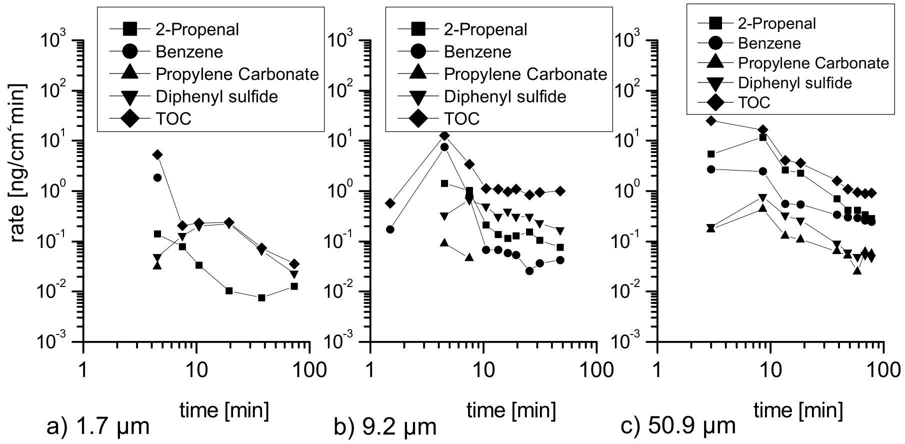

Figure 3.5 *– Outgassing rate as a function of time for three different SU-8 layer thicknesses, a) 1.7 µm, b) 9.2 µm and c) 50.9 µm. For each sample the outgassing rate is plotted for the 4 most abundant components and for the total. The measurements were made using GC-MS, the data points represent the average outgassing rate over a sampling time of 3 min for the two thinnest layers and 5 min for the thickest sample.*

Equation (3.2) shows the conversion from mass to volume-times-pressure using the ideal gas law. In these equations p is pressure in Pa, V is volume in m^3, n is the amount of molecules (in mol), R is the universal gas constant (8.314 $\mathrm{Pa} \cdot \mathrm{m}^3 \cdot \mathrm{mol}^{-1} \cdot \mathrm{K}^{-1}$), T is absolute temperature in K, and M is the molar mass (assumed to be 56 g/mol).

$$
\begin{aligned}
p \cdot V &= n \cdot R \cdot T \\
n &= \frac{m}{M} \\
p \cdot V &= \frac{m \cdot R \cdot T}{M} \rightarrow m = M \cdot \frac{p \cdot V}{R \cdot T} \\
q_{0,pV} &= q_{0,m} \frac{R \cdot T}{M}
\end{aligned}
\tag{3.2}
$$

For the measured rate of 104 $\mathrm{ng} \cdot \mathrm{cm}^{-2} \cdot \mathrm{min}^{-1}$ we find the following.

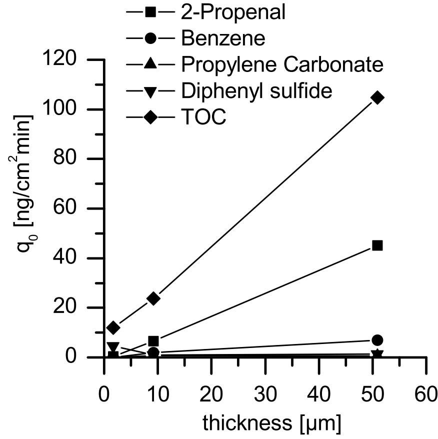

Figure 3.6 *– Values of the linear constant q_0 for different compounds as well as for the total, plotted vs. thickness of the SU-8 layer.*

$$\begin{aligned} q_{0,m} &= 104 \text{ ng} \cdot \text{cm}^{-2} \cdot \text{min}^{-1} \\ q_{0,pV} &= 104 \cdot 10^{-9} \frac{8.314 \cdot 293}{56} \\ &= 4.524 \cdot 10^{-6} \text{ Pa} \cdot \text{m}^3 \cdot \text{cm}^{-2} \cdot \text{min}^{-1} \\ &\equiv 0.573 \cdot 10^{-6} \text{ Torr} \cdot \text{l} \cdot \text{cm}^{-2} \cdot \text{s}^{-1} \end{aligned} \quad (3.3)$$

The level of $0.6 \cdot 10^{-6}$ Torr·l·cm^{-2}·s^{-1} corresponds well to levels known from literature. For polyimides and other polymers values of around $0.8 \cdot 10^{-6}$ Torr · l · cm^{-2} · s^{-1} are reported [107].

Figure 3.6 shows a plot of the level of outgassing rate defined as the offset constant q_0 plotted vs. the SU-8 layer thickness. The almost constant slope suggests that the outgassing can be characterized with a volume emission. If we look at the signal for total outgassing we find the volume emission to be approximately 19 μg · cm^{-3} · min^{-1}.

As mentioned earlier outgassing from some samples show a clear GBL contribution, in other samples however there was little or no GBL found. This indicates that the remaining solvent concentration is not a very well controlled parameter despite strong efforts to keep processing and packaging procedures repeatable. Because the layer thicknesses were all found to be as expected (in accordance with known spin-curves) the starting material must be comparable in all cases. The variation in final solvent concentration might be due to environmental conditions, similar to the results on SU-8 adhesion presented in [79]. The variation

in outgassing rate of heavier, less volatile, compounds like di-phenyl sulfide was found to be much less variable.

The GC-MS measurements are performed over a fairly long period at elevated temperature under normal atmospheric pressure (in a nitrogen ambient). This means the measurement itself is very similar to a hotplate hard-bake at 150 °C. Hard-Bake steps have been discussed previously in section 2.3.4 on page 32. As stated previously the impact of a Hard-Bake on the functionality of the device has to be carefully investigated, but a significant benefit in terms of outgassing characteristics is clearly present. The outgassing rate is inversely proportional to the bake time. From the given plots (figs. 3.5–3.6) we see that at a temperature of 150 °C a Hard-Bake in the order of 10–30 min is very effective to precondition the material for lower outgassing during operation. We see this also from the cumulative plot of total outgassing shown in fig. 3.4b, after 10–30 min most material is released. It is important that the bake temperature is significantly higher than the operating temperature at which the SU-8 structures will be used. Gaseous detectors and vacuum electron multipliers are typically operated at or near room temperature.

Outgassing at room temperature is severely limited, at least when compared with high temperature outgassing. To test the sample handling and storage procedure a set of two identical samples was measured at different times. One measurement was performed straight after fabrication (of both samples). The other was stored for 36 days at room temperature wrapped in Al foil. The stored sample was then measured following the exact same procedure. The measurements were nearly identical, indicating that any possible outgassing at room-temperature did not affect the sample or the amount of volatile components present in it.

3.3 Conclusions

Several methods are used to characterize the release of gaseous species from solid, fully processed, SU-8 layers. The qualitative (MS) and quantitative (GC-MS) measurements lead to the conclusion that a hard-bake of 150 °C is very beneficial for outgassing from SU-8 structures, the outgassing rate is inversely proportional with time.

The outgassing level is comparable to Kapton which is the material used for many GEM foils. This means that integrated Micromegas type gaseous detectors made out of SU-8, such as InGrid, will also behave similar to GEM foils. Ingrid detectors could then be used in applications in sealed chambers where there is a fixed gas ambient that is not flushed during the entire lifetime of the system. Examples of such applications are the sealed detectors shown in [108] and [109].

The main volatile components are benzene, 2-propenal, GBL, propylene carbonate and di-phenyl-sulfide. Further, a strong outgassing signal with mass/charge

of 44 amu/e is identified. Since no measurable amount of propane is found we conclude that this signal is caused by CO_2 originating from decomposition of the material.

The outgassing rate can be checked by monitoring the pressure of a sealed vacuum chamber containing a sample of SU-8. Without knowing the exact composition of the material that is outgassed this experiment could provide an interesting new result. If we assume a chamber of 1 l in volume the pressure rises with approximately $6 \cdot 10^{-6}$ Torr $\cdot$ s^{-1} for a sample of 10 cm^2. In 1 hour this results in a pressure change of $2.8 \cdot 10^{-2}$ mbar. This value is easily measurable, if the sample area is increased further (which is certainly feasible) the pressure change increases accordingly.

Chapter 4

Photon sensitive InGrids: detector design

This chapter deals with the InGrid gaseous detector structure. First we review the device, the technology to construct it and the way it can be combined with readout elements such as CMOS imaging chips. More details can be found in the theses of Max Chefdeville [37] and Victor Blanco Carballo [67]. These reports introduce the InGrid detector and present the first results for electron detection and imaging. This chapter focuses on the optimization of the structure for UV photon detection.

4.1 The detector system

The use of InGrid for photon detection is investigated in two stages. Initial experiments are carried out on test devices with a non-patterned single anode read-out, this work is documented in [110]. All the electronics are external. In the final stage the InGrid structures are constructed onto Timepix CMOS imaging chips, results from this are published in [111]. These chips act as a pixellated read-out anode. The photosensitivity is obtained by coating the grid with a reflective CsI photocathode [112]. CsI is a very robust photocathode that has been used in combination with many gaseous photon detectors [44]. In [113] a Micromegas device with a single anode is coupled to a CsI reflective photocathode. A CMOS imaging chip coupled to a non-integrated gaseous electron multiplier (GEM) with CsI photocathode was described in [54]. The work presented in this chapter differs from the earlier work in that it presents the first fully monolithic embodiment of a UV-photon imaging detector.

The detector comprises of three elements; the imaging chip, the integrated Micromegas grid and a reflective photocathode. In the next sections all elements

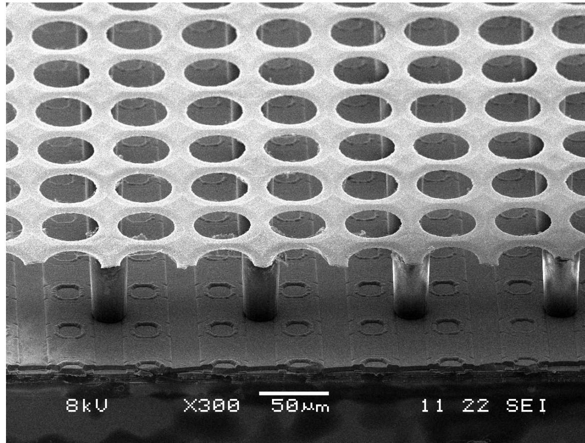

***Figure 4.1** – SEM image of a complete gaseous detector structure with Timepix substrate, highly resistive spark protection layer and InGrid structure with isolating pillars supporting a perforated Al grid. This structure in the state as shown above can be used for electron detection. A photocathode can be added to make it sensitive for photon irradiation.*

will be introduced in detail. Fig. 4.1 shows the gaseous detector assembly before deposition of the photocathode.

4.2 The Timepix CMOS imaging chip

The Timepix chip used here [63, 64] is a variant of the Medipix2 chip [62]. It has been designed by the Medipix2 Collaboration led by CERN. The development of Timepix was paid for by the EUDET project. The Timepix chip contains a matrix of 256×256 square pixels with a size of 55 μm. The total imaging area is $\sim 14 \times 14$ mm^2. Each of the pixels has a metal input pad connected to its own pre-amplifier built into the pixel. The collected charge is read out with a charge sensitive pre-amplifier capable of detecting charges of less than 1000 electrons. The charge is compared with a threshold value which can be changed per pixel. There are different readout modes. Just as Medipix2 the chip can be used to count the number of hits above a threshold during a defined shutter period. In Timepix-mode the arrival time of the first hit above threshold is recorded per pixel and in TOT-mode (Time Over Threshold) the 14 bit counter is incremented as long as the signal remains above threshold. Because the discharge current of the input capacitor is kept constant at a known value the TOT readout can be used to measure input charge [114], and as such each pixel functions as an ADC (Analog to Digital Converter).

The post-processing technology to fabricate the detector structures is entirely compatible with the underlying CMOS devices. Most important in this respect is the maximum temperature during processing. To preserve CMOS interconnect integrity the temperature should not exceed 400–450 °C. The temperature needed to fabricate the SU-8 polymer support structure does not exceed 95 °C. The sputtering process needed for metal deposition has also been found to be compatible with the underlying chips [68]. Other aspects that need to be considered are the preservation of the hydrogen passivation, prevention of charge build up and related device degradation during the course of plasma processing and device degradation due to chemical impurities that can be introduced into the CMOS structure. The last aspect is notoriously dangerous, especially metals such as Cu, Au and Na can have a strong negative impact on device performance. Also other alkali metals such as Cs are dangerous. Especially when CMOS chips are post-processed in more experimental facilities (such as university cleanrooms) exposure to such metals is unavoidable. Thermal evaporation of CsI is a good example of this. The only real solution is therefore to provide good barrier layers to protect the active CMOS devices. Such barriers, often Ta, TaN, Si_xN_y or SiC, are already part of the final stage of the CMOS manufacturing. Some of these barriers are already formed before the interconnect stage of manufacturing to protect the front-end device layer from metals used in modern interconnect (back-end) technology such as Cu. At the end of the total CMOS process (including the interconnect) another silicon nitride based barrier layer is deposited that covers the entire chip except the bondpads formed in the top metal layer. This is the case for our detector chips.

In our experiments we have not noticed any degradation of the CMOS substrates due to the post-processing. In some extreme cases the chips were physically damaged due to the post-processing. In those cases the damage could be attributed to operator errors. Some chips have been electrically damaged during operation of the detectors by the impact of spark discharges that occurred in the detector. This is of course not related to the post-processing.

The post-processing of the chip can be divided in two parts. The first part is the preconditioning of the chip and after that the construction of the actual detector structures is performed. This preconditioning consists of a cleaning step and of the formation of a spark protect layer. Cleaning is done by immersion in a bath of fuming nitric acid (10 minutes in 100% HNO_3 at room temperature), a rinse in deionized water in a so called quick dump rinser (QDR) and spin drying of the substrates under nitrogen. The spark protection layer is deposited to reduce the impact of sparks on the chips during operation of the detector. Following that the InGrid detector structure is fabricated.

4.2.1 Initial post-processing of the chips

The first step is to cover the chip surface with a spark protection layer. This layer is deposited after dicing of the wafers into individual chips. But it can also be performed on larger segments consisting of multiple dies or even on entire wafers. In fact this step can also be done in the facility that processes the CMOS IC rather than the post-processing site. The current best known process [115] is to deposit a very high-ohmic Si-rich silicon-nitride layer onto the entire chip surface. This layer is not patterned across the pixel matrix but the deposition is masked so that the IO bondpad areas at the edge of the chip remain uncovered. Figure 4.7 (left) shows a chip (in a later stage, after bonding) with the silicon-nitride layer (grey) covering the pixel matrix whereas the bondpads at the top of the chip (green) are not covered. The layer is deposited by plasma-enhanced CVD, the devices presented in this thesis all have a protection of 7 μm thickness.

The highly resistive layer protects the chip in the case of discharges that can occur in the gas layer above the chip, in the detector. The spark protection layer acts by quenching the spark before the built-up charge becomes too large. At the location of a possible spark, due to a field peak for instance, a charge build up at the top surface of the highly resistive layer is created. The dipole field of this charge immediately reduces the electric field and prevents a large discharge current to occur, such a discharge would otherwise usually kill the IC. Signal transport through the layer is unaffected because of immediate charge mirroring. Charge deposited on the top surface is mirrored with an image charge at the bottom side, which is connected to the pixel input pad. More details can be found in [115].

4.3 The InGrid structure

The InGrid gaseous detector structure is a suspended metal grid placed over the anode readout plane. The grid is made out of Al, it is supported by isolating pillars made out of SU-8, a polymer photoresist material that is very strong and very suitable for permanent structures. The manufacturing process is illustrated in fig. 4.2 and described in detail in this paragraph. The first panels of fig. 4.2 show the starting material and the deposition of the spark protection layer.

A photoimagable SU-8 polymer layer is spin cast onto the substrate (fig. 4.2c). This layer is baked on a hotplate at a temperature of 95 °C to render it solid. In some cases a 1 μm thick photoresist layer is added at this stage (fig. 4.2d), this will be explained later. The layer is imaged with broadband UV light using a mask that defines the pillars, fig. 4.2e. The lithography is a performed in a contact aligner to provide < 1 μm alignment error between the pillars and the anode pattern. A dark field mask is used, SU-8 is a negative photoresist, the parts that are exposed are cross-linked through a chemically amplified process initiated by a photo sensitive

acid that is part of the resist. After exposure the substrates are baked at 80 °C to enhance the cross-linking. The layer is not yet developed, this is where the processing deviates from conventional use of SU-8. Instead the unexposed regions of SU-8 are used as a sacrificial layer to support the grid metal.

A 1 μm thick Al layer is sputtered onto the imaged SU-8 layer using magnetron DC sputtering at high power (7 kW) and high rate (> 800 nm/min), see fig. 4.2f. To form the perforated grid the metal is patterned using lithography, wet etching in PAN etchant [92] at room temperature, QDR and spin drying, the result is shown in fig. 4.2g. The resist on top of the metal is not stripped separately, instead it is removed during the development of the SU-8 layer. The metal is etched at room temperature in order not to initiate further cross-linking of the SU-8 regions between the pillars. For the same reason the photoresist needed as the etch mask for the metal pattern is not baked at elevated temperature. Instead the photoresist is dried at a mild temperature (30 °C) during an extended period.

The SU-8 layer, which has been imaged earlier, is then developed in acetone, removing the unexposed, uncross-linked material from below the grid through the holes in the metal, fig. 4.2h. The structure is rinsed by immersion in isopropyl alcohol, this is also done in between successive acetone soak steps to prevent delamination of the structure. After drying the structure appears as shown in fig. 4.1. Our present detector has 25 μm diameter holes at a pitch of 55 μm; the multiplication gap (grid-to-anode) is $\sim$80 μm. In section 4.4 further details are given on the geometry optimization.

During sputtering of the metal it is found that in some cases a thin skin of cross-linked SU-8 is created in between the pillars. This is the result of exposure of the photoresist by the plasma used for sputtering as well as by the heat that is deposited into the layer during this step. It is known that SU-8 can be cross-linked also by heat. The skin created underneath the metal is problematic during the development step. To alleviate this problem a buffer layer is introduced. This is a layer of Oir 907-17[1] positive tone photoresist of 1.7 μm thickness. This layer is deposited by spin coating after the SU-8 layer is made and soft-baked, as shown in fig. 4.2d. An additional bake is performed to cure the positive photoresist. The two resists are imaged together. Because the Oir layer is a positive-tone photoresist, the material is removed at the location of the pillars. The resist is developed in its dedicated developer (an aqueous base solution that does not influence the SU-8) before the deposition of the metal. The rest of the buffer layer (beneath the metal) is removed when the SU-8 is developed, the photoresist is highly soluble in acetone.

The InGrid structure (as well as the silicon-nitride charge protection layer) are only present over the area of the pixel matrix. The charge protection layer is

[1]Fuji Film Electronic Materials

patterned during deposition using a shadow mask. The InGrid processing and the lithography masks are designed so that the structure is only constructed in the pixel region. The top part of the chip remains uncovered. This area contains peripheral electronics needed for the readout of the pixel information and the IO bondpads. These are kept bare so that wire connections can be made to them. The two areas are schematically drawn in panel i) of fig. 4.2.

4.4 InGrid geometry

The size and the spacing of the grid holes has a large influence on the response of the detector. Only the metal grid area in between the holes is coated with a photocathode and only this surface is photon sensitive. Photons that fall through the holes do not lead to detected signals. Even if these photons convert into a primary electron at the anode surface beneath the hole, these will not be amplified. A larger hole size will decrease the detector response. In this respect it pays off to decrease the hole size as much as possible. At the same time there are two effects that limit the minimal hole size.

First of all the hole size cannot be made arbitrarily small due to technological reasons. A smaller hole size leads to more complicated development. The transport of solvable SU-8 from below the grid through the holes is hindered, this leads to SU-8 remains below the grid even after extended development. Furthermore during deposition of the metal grid on the already imaged SU-8 the top part of the SU-8 is crosslinked. This is due to radiation and heating of the resist that occurs during the sputter deposition of the metal. The result of this is a thin skin of cross-linked SU-8 that covers the holes in the grid. The additional buffer layer of positive photoresist beneath the metal grid, see fig. 4.2d, reduces this problem but it does not eliminate it entirely. At the development step this skin has to be broken through and removed by subsequent washing in acetone and isopropyl alcohol baths. The smaller the diameter of the holes the more difficult it becomes to pierce the SU-8 skins. In practice a minimal hole size of $\sim$15 μm is needed for successful development.

Another limitation for the hole size stems from the field distribution around the grid. For successful extraction of primary electrons from the photocathode surface it is needed that there is some transverse electric field to 'pull' the electrons out of the photocathode material and emit them into the gas. The extraction field needed to achieve good extraction efficiency from a solid photocathode into a gas medium depends on the gas mixture and on the temperature and pressure; it is generally a few kV/cm. The extraction efficiency was tested experimentally for the gases used with our detector. Good efficiency is achieved from around 1 kV/cm, all experiments were carried out at atmospheric pressure, so this limit corresponds

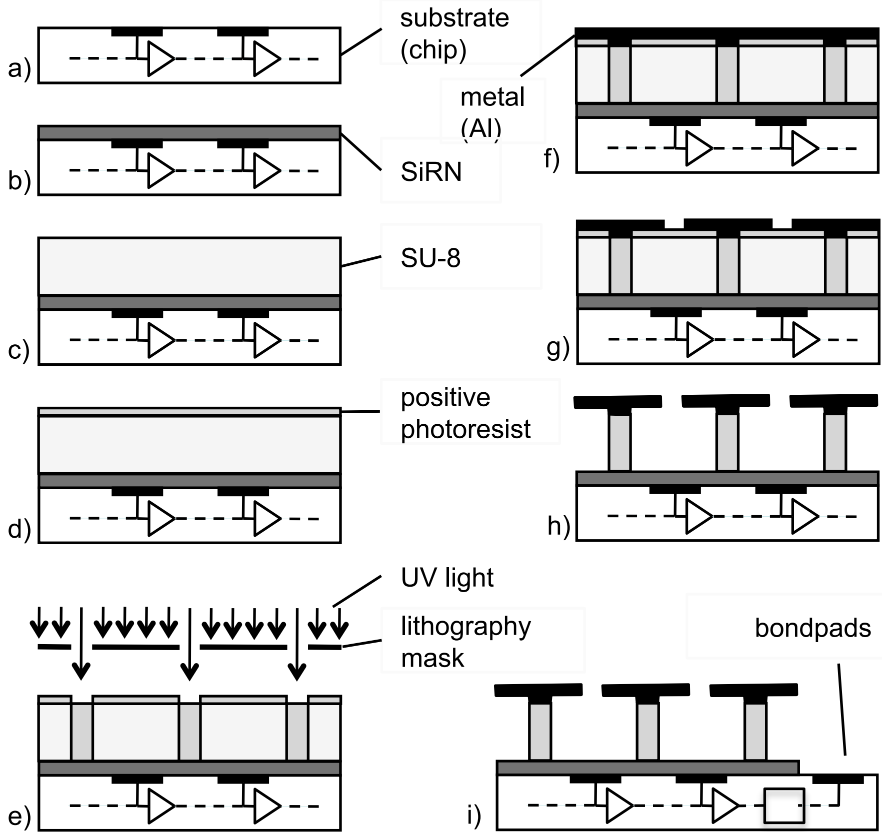

Figure 4.2 *– Process flow for the InGrid structure. a) The substrate can be a CMOS imaging chip, a wafer, or any other substrate. b) A Si rich nitride (SiRN) layer is deposited on the surface for spark protection. c) An SU-8 layer is spin-cast and baked. d) A thin layer of positive photoresist is deposited as a buffer layer against unwanted SU-8 crosslinking. e) The SU-8 layer is imaged using a mask. The exposed regions of the SU-8 become cross-linked, the positive resist is developed. f) A metal is sputtered on top of the imaged SU-8 layer. g) The metal is patterned into a grid using lithography and wet etching techniques. h) The SU-8 support structure is developed in acetone and rinsed in isopropyl alcohol, the unexposed SU-8 is removed in the solvent through the holes in the metal grid layer. i) Final situation showing that the region of the IO bondpads remains uncovered.*

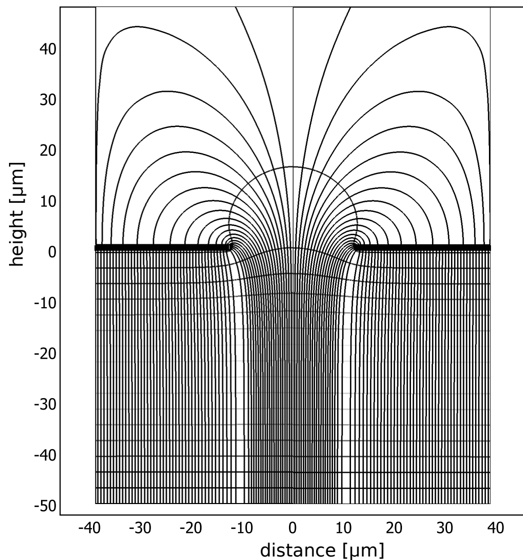

Figure 4.3 *– Field distribution around an InGrid pixel. This plot was extracted from simulations made with Comsol Multiphysics [118].*

to around 1.3 V/cm·Torr. Further details can be found in section 4.7.3. This is in line with reports of earlier work on CsI photocathode extraction efficiencies, reported values are in the range 1–2 kV/cm [116, 117].

In our application the cathode mesh placed above the grid is only used for shaping the field in the drift region, this shield prevents electrons from drifting away from the grid. The bias on the cathode is the same as that applied to the grid. In other words the externally applied drift field is zero. The electric field distribution seen at the top surface of the grid is therefore solely the evanescent field of the high field region below the grid (the multiplication field). Figure 4.3 shows the field distribution around an InGrid pixel. The field strength across the grid surface drops further away from the holes. At a given hole pitch (as dictated by the chip readout) a certain minimal hole size needs to be maintained before the electric field in between the holes (furthest from the holes) drops below the extraction limit. If this happens that part of the photocathode becomes less responsive, essentially limiting the effective efficiency of the photocathode.

To predict the trade-off quantitatively a simple model is made. We simulate the transverse component of the electric field above the surface of the grid using finite element calculations with Comsol Multiphysics [118]. The field is highest over the area of the holes, where it is closer to the electric field below the grid, in the multiplication region. Away from the hole the field strength drops. We assess the

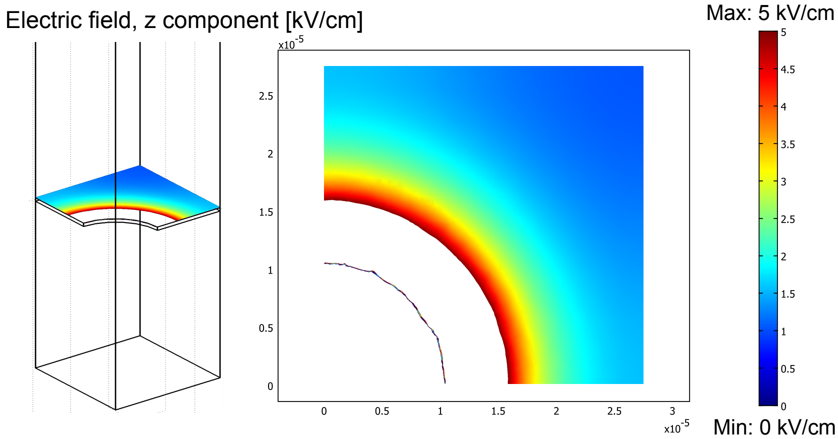

Figure 4.4 *– Illustration of the simulation space and the field distribution on a horizontal plane just above the grid. The simulation space is reduced to a quarter of one hole using symmetry considerations.*

electric field strength along the line from one grid hole to the next. The left part of fig. 4.4 shows part of the simulation space and the structure, the area above the grid extends much further. By setting the boundary conditions of the simulation space such that the field distributions are symmetrical (mirrored) a quarter of the grid unit cell is sufficient to construct the electric field distribution across the entire device. The right panel of the figure shows the electric field strength distribution in the horizontal plane just above the grid. In this image we see that the field strength drops off farther from the grid hole; the field strength is truncated at 5 kV/cm. We can now plot the electric field strength along a line in this plane from the center of the grid hole to the opposite corner. This is the extraction field strength needed to allow photo-electrons to exit the surface of the photocathode into the gas medium. These field profiles are plotted in fig. 4.5 for different hole diameters. The hole-to-hole pitch is always the same, 55 μm, in a square layout, this is the geometry of the Timepix readout chips. The field profiles are plotted against the distance from the hole, up to the midpoint between two holes (at approximately 39 μm). The bias potential applied to the grid is 500 V, the field strength scales linearly with the bias voltage. The gap height of this structure is 75 μm.

For a given bias potential we determine the distance from the hole where the field strength drops below a chosen limit for each of the field profiles. For this assessment we have checked for limits of 0.5–2 kV/cm. We assume that the part further away, where the field strength is below the limit, is not generating any primary electrons. This blind area determines the loss of effective photocathode

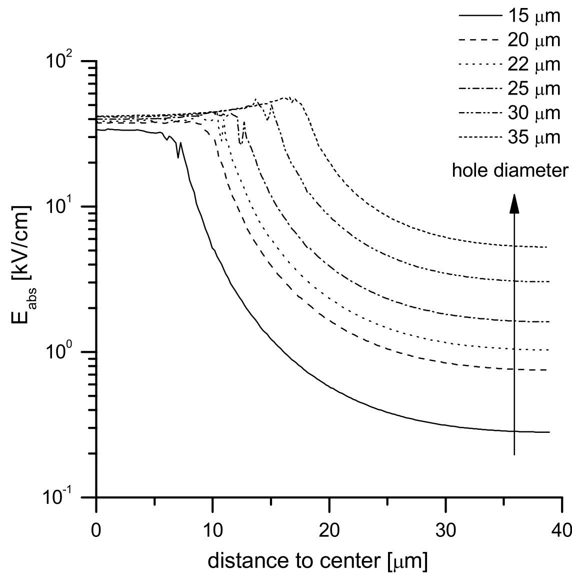

***Figure 4.5** – Transverse electric field strength above the grid for various hole sizes (as indicated in the legend). The horizontal axis shows the distance from the center of the hole. The nearly constant field strength up to the edge of the hole is comparable to the field strength below the grid. Away from the hole the field strength drops rapidly*

area. We can then compare this with the drop in efficiency due to the area occupied by the holes. In both cases we assume that the efficiency varies linearly with the effective area of the photocathode. In other words, we assume an ideal transfer efficiency of the electrons as they are transported into the holes.

Figure 4.6 shows a plot of the efficiency trade-off for a set of limits. The relative efficiency is plotted on the vertical axis against the hole size on the horizontal axis. The line labelled 'OT' is the efficiency loss only due to the optical transparency of the grid. The other lines show the efficiency loss when different extraction limits are used. For small holes we see a sharp drop in efficiency due to increased dead-area in between the holes. There is an optimal hole size where the efficiency peaks (at levels of 80–90%), for larger hole diameters the area loss due to the optical transparency quickly dominates. With an extraction limit at 1.5 kV/cm field strength the optimal hole size is 25 μm. This is the hole size that is used in all experiments. In section 4.7.3 the extraction of photoelectrons in different gas ambients is characterized. A field strength of ca. 1 kV/cm is required for efficient extraction of the primary charge carriers.

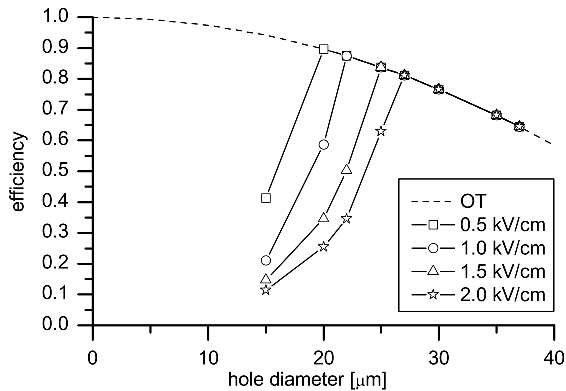

Figure 4.6 *– Efficiency loss for an InGrid device with varying hole size. The holes are placed in a square layout with a pitch of 55 μm, the detector is intended to be coupled to a Timepix chip. The data labelled OT shows the loss purely due to the increased optical transparency of the grid. The other curves also include the loss due to the formation of a blind, non-responsive, zone in between the holes.*

4.5 Detector integration and operation

After post-processing the chips are bonded to a readout board. Figure 4.7 shows a bonded chip on the readout board, this PCB contains all the circuitry to connect the chip to external devices and to apply the right bias conditions to power the chip. The CsI photocathode is deposited by thermal evaporation onto the detector surface after bonding of the InGrid devices. The photocathodes are typically 200 nm thick. The process after InGrid manufacturing is illustrated in fig. 4.8.

The bonded chip can be readout by connecting the board to a readout module, the module fits into a parallel connector attached to the board. In most cases we have used the USB module developed by the Technical University of Prague. This is a small box of $4 \times 5 \times 2$ cm^3 that is connected with the board. It interfaces the chip, via the readout board, with a PC connected with a USB connection. Bias voltage for the chip is also supplied from the USB connection. The readout is done from the PC using the Pixelman software, developed by the same group that made the USB readout module [119].

The readout PCB is coupled to a gas tight chamber of approximately $10 \times 10 \times 1.5$ cm^3. This chamber is pressed onto the PCB using screws, a Viton ring is used to seal the interface. The gas chamber has inlet and outlet ports to flush and fill the chamber with controlled gas mixtures. The gases come from bottles and are fed into the chamber using mass flow controllers to set the correct mixture. The

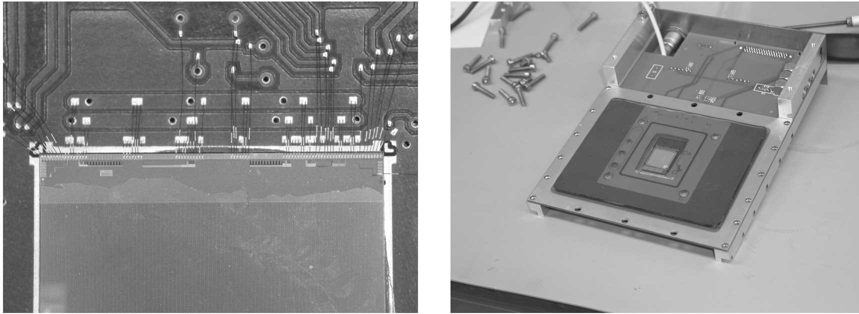

Figure 4.7 – Photographs of a chip bonded to its readout board. The left image is a close-up showing the individual bondwires that connect to the IO-pads of the IC. The image on the right shows the entire board, with chip, and parts of the chamber assembly that is constructed on top of it.

outlet ports are connected to an exhaust through a silicone oil bubbler to prevent contamination of the chamber due to gas back flow. After the chamber is sealed it is first flushed extensively with the chosen gas mixture using a high flow rate. Only after this the detector is used under high voltage.

The high voltage is applied to the detector grid and the mesh cathode using feedthroughs on the readout PCB. The PCB also contains series resistances (of 1 MΩ) and decoupling capacitors for the high voltage connections. The detector bias is applied carefully by slowly ramping up the voltage on the HV source. This is done to prevent high currents due to charge up effects and to be aware of early breakdown of faulty detector structures.

Inside the volume of the gas chamber an additional steel cathode mesh is mounted 5–10 mm above the grid. This mesh is used to control the electric field around the detector. Above this mesh, centered on the location of the chip, is a UV transparent Suprasil quartz window to allow light to reach the detector. A drawing of the entire system is shown in fig. 4.9. The photograph in fig. 4.10 shows the full assembly.

The operation principle of the detector is shown in fig. 4.11. Light impinges onto the photocathode layer on the top surface of the grid. The chip surface (anode) is grounded. The cathode mesh and the grid are typically biased at the same negative potential to prevent photoelectrons to drift upwards. The electrons follow the evanescent field from the high field region below the grid. After drifting through the holes the charge is multiplied towards the anode. This happens through field induced ionization of gas molecules by the drifting electrons, just as in a Geiger-Müller counter or an MWPC. This process is called avalanche multi-

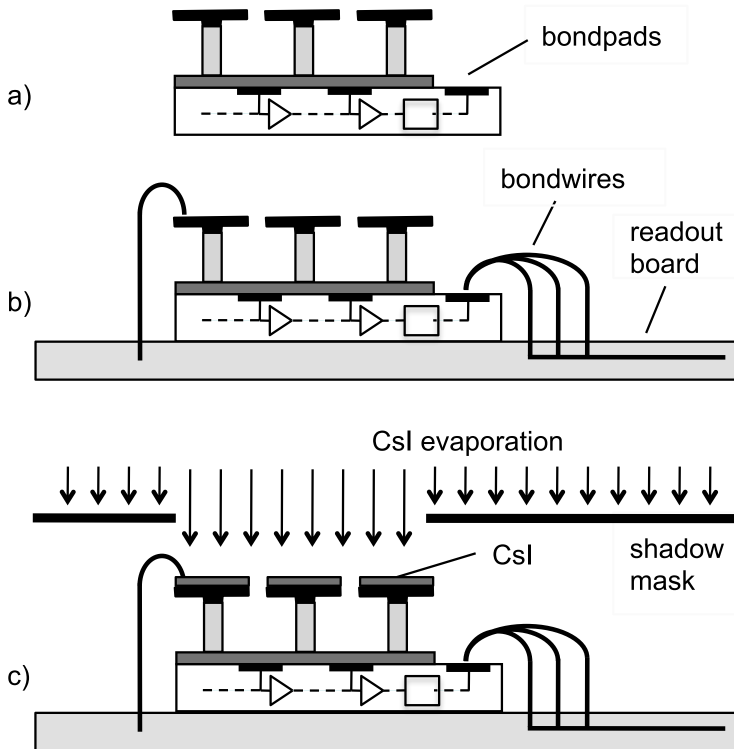

Figure 4.8 *– Final stages of processing. a) Shows the completed InGrid structure on a chip, the spark protection layer beneath the pillars does not cover the outer bondpads. b) The chip is glued to a specifically designed PCB and the chip is connected using bondwires, the grid is also connected to a terminal on the PCB using wirebonding. c) A CsI photocathode is deposited onto the assembly by thermal evaporation. A shadow mask is used so that CsI is only deposited onto the sensitive area of the detector; other areas such as the region for the wirebonds and the rest of the PCB are protected.*

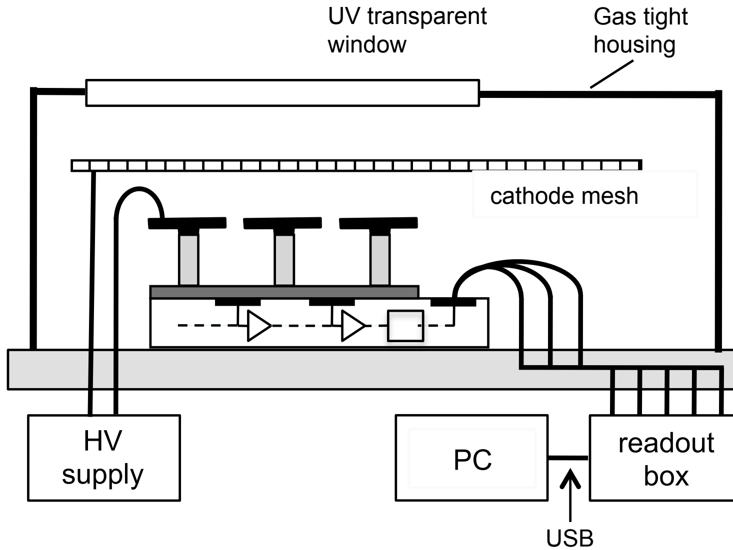

Figure 4.9 – *Drawing of the complete setup. The detector is mounted under a UV transparent window. A steel cathode mesh (of high transparency) is mounted directly above the detector. The PCB contains all the electronics and feedthroughs to bias and read out the chip as well as supply the high voltage connections to the detector grid and the mesh cathode.*

plication. More details can be found in the introduction (section 1.1.3) or directly in the sources referenced there such as the overview report [36] or, more specifically for the InGrid device, the thesis [37]. The charge cloud then falls onto one of the pixels of the matrix.

4.6 The CsI photocathode

To improve the light sensitivity of the detector system a dedicated photocathode is deposited on the grid surface. We use a CsI layer of ca. 200 nm thickness. Such a thick layer acts as a reflective cathode. Photoelectrons are emitted from the illuminated surface and are then transferred to the electron multiplier.

Photoelectrons are created in the photocathode due to the photoelectric effect. If the incident photons have a high enough energy a photoelectron is created. There are other phenomena that influence the overall efficiency of the photon to electron conversion such as the reflectivity of the surface, the penetration depth of photons and the transport of electrons in the bulk of the photocathode to the

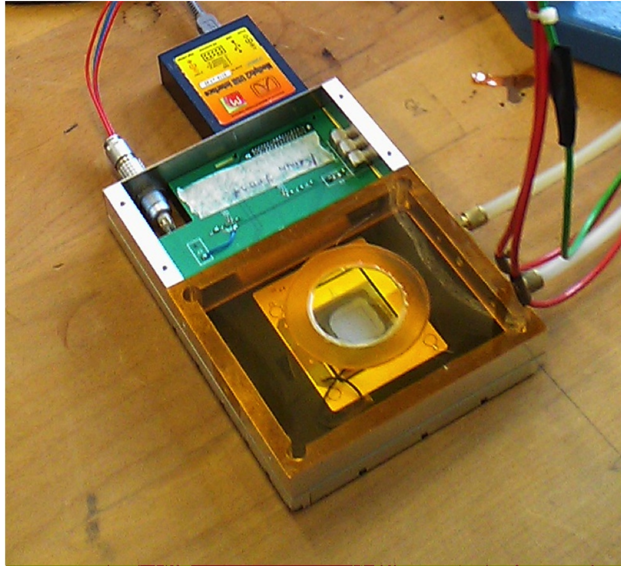

Figure 4.10 – Photograph of the measurement system. In the middle of the chamber is the UV transparent quartz window. The detector can be seen as a vague grey square underneath the steel cathode mesh. On the right side of the chamber are the gas in- and outlet ports. The USB readout module is the small blue box attached to the short side of the PCB, to the left of this are the wires for the high voltage connections.

surface. Electrons can be lost due to recombination or they can lose too much energy to be able escape the surface.

A good photocathode should have a low energy barrier for the creation of electrons. For metals this barrier is called the workfunction, this is a material property. For semiconductors and dielectrics the barrier is the energy step from the Fermi level to the vacuum level. This means, for intrinsic materials, the barrier comprises half of the bandgap and the energy step from the conduction band to the vacuum level known as the electron affinity. For most materials a low work function implies also a low ionization potential; these materials form chemical bonds more easily. In other words, they are more reactive. Many efficient photocathodes are therefore very sensitive and can only be created and operated in a very good quality vacuum ambient.

This means that many photocathodes are not suitable for use with gaseous photocathodes. Others can operate in the gases used for such detectors but they cannot be exposed to air, implying that deposition and detector operation have to

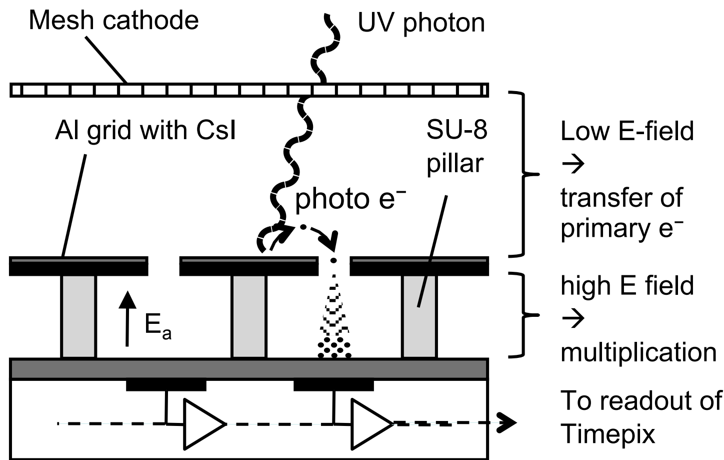

Figure 4.11 *– Illustration of the device and its operation. Light enters through a window from the top; photoelectrons from a CsI photocathode on the grid are focused into the multiplication gap; the resulting avalanche induces charge onto the CMOS pixel array of the Timepix chip — via a discharge-protecting film. Operation is in gas flow mode at 1 atm.*

be performed in a sealed installation with full control over the ambient. To prevent such complicated measures one has to look for the few photocathode materials that are more forgiving, CsI is one of the few such exceptions.

CsI is a very robust photocathode that can withstand exposure to dry air and many other (dry) gases. The layer will, over time, get damaged when exposed to moisture. CsI is hygroscopic, exposure to normal air therefore has to be minimized or it might eventually decompose the photocathode. The CsI layer will dissolve when exposed to moisture, it will recrystallize into a rough non-continuous layer with strongly degraded photoelectric properties [120].

For this reason the deposition is done as the last step, after mounting and bonding of the chip. The whole assembly without the top cover, window and cathode mesh is placed inside an evaporation chamber. The deposition is done by thermal evaporation in vacuum from a solid CsI source using resistive heating [112]. In some cases the CsI layer is patterned using a simple Al foil shadow-mask during deposition. The typical CsI thickness is 220 nm. During deposition the growth rate and layer thickness are monitored using a system with a sensor placed near the substrate. The system senses mass gain of a vibrating crystal, it is calibrated for CsI evaporation.

After deposition the device is removed from the vacuum chamber. The photocathode is only exposed to air during venting, transport, and during the time

needed for mounting the cathode mesh and installing the gas chamber cover. Once this is done the chamber can be flushed with gas. Any dry gas will suffice to preserve the photocathode condition; usually the measurement gas is used. After 1 hr of flushing the flow can be reduced to a low setting, the chip is kept under gas during the entire measurement series.

There is a large variation in claims as to how long CsI can be exposed to air without significant degradation. One possible explanation for these variations is differences in layer morphology. Another likely explanation is the large variation of humidity conditions experienced across laboratories, depending on geographical factors. Some reports claim that a 1 hr exposure to air can already have strong negative effects [120]. Other sources show that the effects of exposure of 24 hours or more is not significant [112, 121]. We have optimized the procedure so that exposure is limited to ca. 10 min. Such a delay is known not to have a significant impact.

4.6.1 Wavelength dependence

CsI responds mainly to deep UV radiation. For wavelengths above 200 nm teh quantum efficiency drops to very low levels [112]. To improve the sensitivity to visible light would require entirely different photocathodes such as bialkali materials [122]. These photocathodes are much more sensitive to ambient parameters making their integration more complicated

The entrance window above the structure (shown in figs. 4.9 and 4.10) is made out of Suprasil quartz glass[2]. This material is transparent to light with a wavelength down to ca. 170 nm. This means only photons with a wavelength in the range 170–200 nm can be detected with our system.

The transmittance of UV photons through the gas layer, between the entrance window and the photocathode, also depends on the gas composition. This is discussed further in section 4.7.3.

4.7 Measurement methods

Using the software to operate the IC the system can be used for imaging. Parameters such as acquisition time and readout mode can be set. We have also used the chip based systems for non-imaging experiments, in which case the chip readout is not used. Apart from the chip based detectors we have also done measurements with devices built onto single anode test devices. We will briefly introduce these devices and the methods used to characterize them. Furthermore we will discuss the choice of the measurement gas.

[2]Suprasil 1 from Heraeus Quarzglas GmbH

The UV light that is detected is from a Oriel model 6035 Ar(Hg) lamp. The light flux is attenuated by placing semitransparent GEM foils in the beam path. The lamp is also placed at a large distance, ca. 50 cm, in front of the entrance window of the chamber. For the imaging experiments the light reaching the detector is patterned using a shadow mask. This mask is placed on top of the window. The mask is made out of a 300 μm thin sheet of stainless steel patterned by laser cutting.

4.7.1 Pulse measurements with chip based detectors

If the anode plane readout of the chip is not used we can readout signals from the grid electrode. For this purpose a dedicated pre-amplifier is included on the readout PCB. The charge sensitive amplifier, with an appropriate peaking time, is connected to the grid. The peak height of the output voltage is correlated to charge. The output pulses are further amplified and shaped using an Ortec 570 Timing Filter Amplifier. The signal is then analyzed using an Amptek 8000A Multi Channel Analyzer (MCA). This system records peak heights of each pulse and a histogram is created of all pulses sorted by charge (in a specified bin size), the acquisition time can be varied at will or it can be stopped after a certain amount of pulses is reached.

The amplification chain can be calibrated for input charge using a dedicated input electrode of the amplifier. This input is connected to the charge sensitive amplifier through a capacitor with known capacitance. By applying voltage pulses from a source we can inject known amounts of charge into the amplification chain and measure resulting pulse height spectra on the MCA. The pulse height spectra can then be calibrated for charge. The relation between pulse height on the MCA (measured in channels) is linear with input charge.

One important element in recording pulse height spectra is noise. Noise pulses are picked up due to ambient light falling onto the detector, other (cosmic) radiation leading to electrons being created in the gas, the bias voltage sources or the charge-sensitive pre-amplifier itself. Before a measurement is recorded a test measurement is made without any input signal, i.e. with the light source turned off. Ideally such noise spectra are recorded for each bias setting, or at least for the lowest and highest bias used, and for each gas choice. The pulse counts recorded during illumination can then be corrected for noise by deducting the noise count from the raw data.

4.7.2 Test devices with a single anode

Devices with a single test anode are made on small 22×22 mm^2 Si substrates where the anode is a large Al pad of 20 mm diameter. On these substrates an

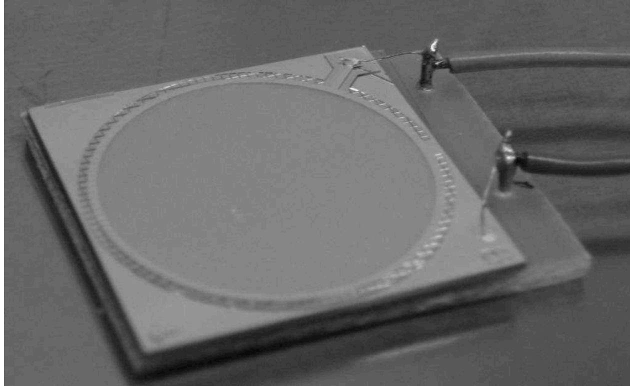

Figure 4.12 *– Photograph of single anode test devices. The InGrid structure is circular, the diameter is 20 mm. These devices are placed in the measurement chamber, the chamber has feedthroughs for the electrical connections.*

InGrid structure is made. The process is the same as that discussed in section section 4.3. After completing the InGrid the devices are glued to a small piece of PCB material and wire connections are made to the InGrid electrodes (grid and anode). The assembly is shown in fig. 4.12. Device operation is the same as for the chip based detectors.

In addition to measurements of pulse height spectra these test devices can be used for current mode measurements. If the photon flux is high and the charge flow to the anode is large one can directly measure this current using a Keithley 610-C picoammeter.

4.7.3 Gas choice

The devices can be operated with different gas mixtures. All experiments so far have been carried out at room temperature and with gas ambients maintained at atmospheric pressure[3].

In initial tests on single anode devices (not imaging chips) we observed good results with both $Ar-CH_4$ and $Ne-CH_4$ mixtures. These devices are inherently spark proof. Sparks might occur but they do not have detrimental effects because the single large anode is robust, the readout is also not impacted by the charge deposited by a spark.

[3]To prevent reflow of the gas back into the chamber a silicone oil bubbler is connected between the chamber and the exhaust. The associated flow resistance requires that the pressure in the chamber is actually slightly higher than atmospheric. This small difference (in the order 10–20 mbar) is not important for these measurements.

The devices made using imaging chips as readout plane are more vulnerable. Best results were obtained with a He/isobutane (80/20) mixture. Device operation is very stable in He/isobutane, several detectors have been operated for up to several weeks without any signs of degradation. Lower gains were reached in Ar based mixtures. The devices were also not operating stably in this gas and eventually broke down due to spark discharging. Using He/isobutane prevents this problem because of the strongly reduced ionization constant in He [36]. There are two drawbacks related to the use of He and isobutane. First, isobutane absorbs UV radiation. For our setup this effect is limited because of the low isobutane concentration and the small thickness of the gas layer ($\sim$1 cm). Secondly, in He there is rather high backscattering of photoelectrons on gas molecules compared to other noble gases [116]. This reduces the effective quantum efficiency of the detector, even when mixed with isobutane.

Fig. 4.13 shows measured extraction efficiency into various gases; the efficiency is the ratio between the extraction levels in gas and in vacuum, at the same bias and irradiation conditions. In He/isobutane (80/20) we reach an extraction level of around 50% for normal operating conditions ($\sim$ 2 kV/cm). For backscattering in other gas mixtures see [117].

Although the extraction levels reached in He/isobutane are sufficient for many types of experiments it is interesting to see whether the gas choice can be optimized to give higher extraction efficiency. To reduce the risk of sparking the discharge protection layer thickness can be increased. We have used a thickness of 7 μm. Recent results indicate that much better results can be obtained with thicker layers of up to 15 μm [115]. It is interesting to see if this allows operation in gas mixtures based on Ar or Ne.

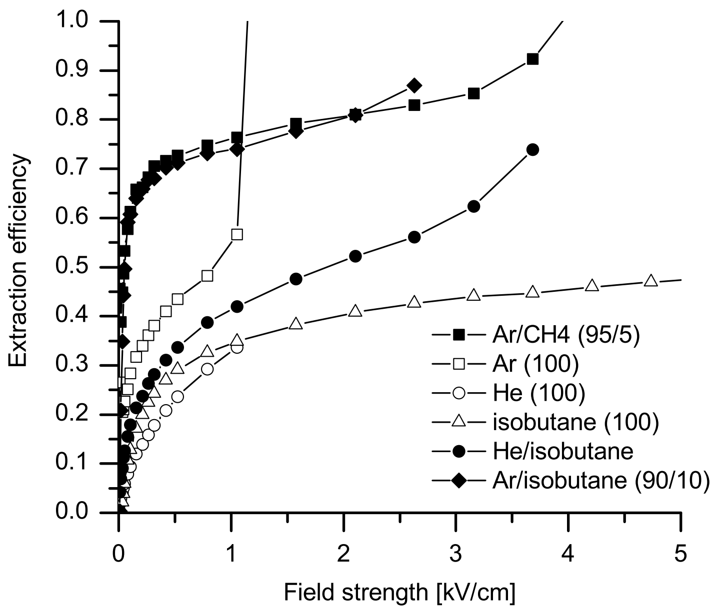

Figure 4.13 *– Extraction efficiency of photoelectrons from a CsI photocathode into various gas mixtures (reference to vacuum). All gases were maintained at 1 atm. The extraction is plotted against the field strength in the drift gap above the photocathode surface.*

4.8 Summary

This chapter presented the InGrid gaseous detector and its use for photon detection. A dedicated photon sensitive layer is added to the detector structure to make it an efficient detector. Two types of test devices were introduced and fabricated, devices with a single, large, anode and devices were the anode is an array of charge sensitive pixels. The first device will be used for initial characterization, the latter device will allow to do imaging experiments. The InGrid geometry has been optimized for efficient transfer of primary charges. The measurement methods that are needed have been introduced. In the next chapter results obtained with photon sensitive InGrid devices are presented.

Chapter 5

Photon sensitive InGrids: experimental results

5.1 Photon detection without a dedicated photocathode

After the grid structure is made and the chips are bonded to the detector, it is already operational. It can be used for detection of free electrons, for instance from conversion of radioactive radiation in the gas above the grid. It can also be used to detect photons by means of the photo electrons created at the Al grid surface. The quantum efficiency of this conversion is however very low compared to the situation with a dedicated photocathode. We used this method to initially test devices before experiments with deposited photocathodes.

The device has a 80 μm avalanche gap height, the hole size is 25 μm with a hole pitch of 55 μm. The detector is operated in He/iC_4H_{10} (volumetric ratio 77/23). The detector is illuminated with a D_2 lamp placed far away from the detector. There is a mesh cathode placed 2 mm in front of the grid. This electrode is biased at the same voltage as the grid to optimize the collection of primary charges from the photocathode and to electrostatically shield off the drift region above the grid.

Figure 5.1 shows a gain curve of the device under test. The gain is measured by measuring the charge of signals from the conversion of ^{55}Fe x-rays in the gas volume above the grid. The ^{55}Fe source emits 5.9 keV photons, when these interact with the gas atoms in the space above the detector an amount of electrons are generated. The distribution of the created charge depends on the gas species. In He the primary charge has a mean value of 160 electrons. The charge that is created drifts towards the grid and is then multiplied by the detector. The charge pulses are recorded using a charge sensitive amplifier that is calibrated before hand by injecting known charges with a capacitor and a voltage pulse generator.

Figure 5.2 shows images obtained in He/iC_4H_{10} (77/23) using Medipix mode

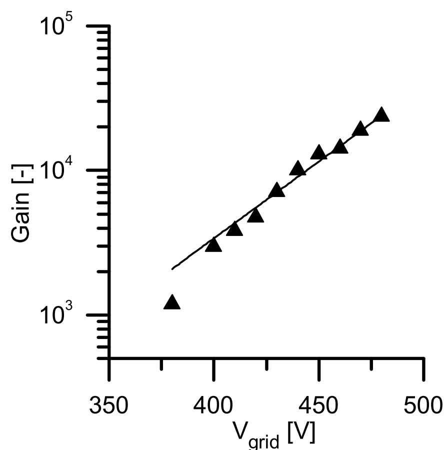

***Figure 5.1** – Gain curve for the initial tests with an uncoated InGrid, He/iC_4H_{10} (77/23), measured using charge from the conversion of ^{55}Fe X-rays in the drift region of the detector.*

counting under UV-photon irradiation, the acquisition time is 300 s. The bias voltage is 480 V, this corresponds to a gain $G \sim 2.7 \times 10^4$. The fingerprint image was recorded without CsI on the Al grid. This shows that, in spite of the (very) low quantum efficiency, even without CsI the detector performs as a UV imaging device. The left part of fig. 5.2 shows an empty reference frame, the window of the detector was cleaned just prior to taking this empty frame. Next a fingerprint impression was intentionally made on the window[1] and another frame is recorded, this is the middle image. The frame of the negative fingerprint was recorded with the same conditions as the reference frame. The third frame in the illustration is the result of subtracting the fingerprint frame from the reference frame. The subtraction is done element-by-element over the whole pixel matrix, the image is also rotated over 180°, to yield the positive fingerprint image on the right of fig. 5.2.

The leftmost panel of fig. 5.2 (the empty reference frame) shows an interesting periodic pattern. This is the result of interference between the mesh cathode and the chip. This effect is discussed in more detail in section 5.3.5.

Figure 5.3 shows two images recorded by placing a steel shadow mask in front of the detector window. Both images are recorded in Medipix mode with an acquisition time of 300 s, the bias voltage was 480 V.

[1]The print was made by the right index finger of Martin Fransen.

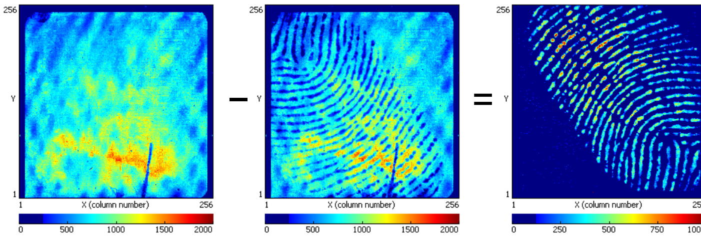

Figure 5.2 *– A fingerprint image intentionally left on the detector window. The left frame shows an empty reference frame, the middle frame is recorded after a fingerprint is intentionally left on the detector window*

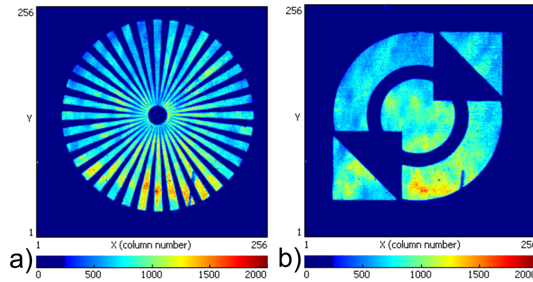

Figure 5.3 *– Two images of UV radiation recorded with an uncoated InGrid device, a) a Siemens star and b) the logo of the University of Twente. Both images were formed by placing a steel shadow mask in front of the detector window.*

5.2 Results with single anode detectors

Initial tests on the combination of InGrid detector structures with CsI photocathodes were performed on test devices without the chip readout (see also section 4.7.2 and fig. 4.12). Instead the readout was done using a single, unpatterned anode. The study was carried out with small circular InGrid detector prototypes of 20 mm diameter. There was a continuous SU-8 polymer wall around the edge of the detector to prevent discharges. The active inner part of the detector was 18 mm in diameter. The holes in the metal grid had a diameter of 13 μm and a pitch of 20 μm. The grid-to-anode amplification gap was 80 μm. The grid was coated with a 200 nm thick CsI reflective photocathode. A cathode mesh to control the electric field in the drift space is placed 5 mm above the grid. The assembly is exactly as shown in figs. 4.9 and 4.11, except that the substrate is not a CMOS chip but an unpatterned Al substrate.

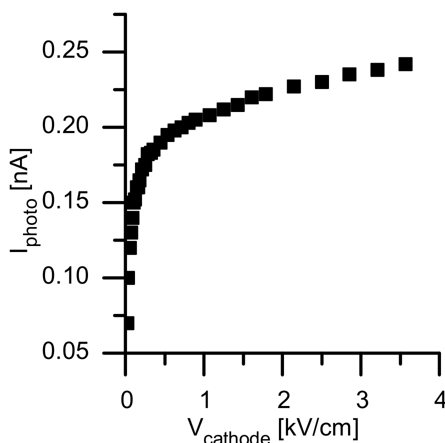

***Figure 5.4** – Photocurrent extracted from the grid of the detector under UV irradiation, measured in Ar/CH_4 (95/5).*

5.2.1 Current mode measurements

Figure 5.4 shows the photocurrent extracted from the cathode when it is illuminated with UV radiation. The current was extracted from the grid towards the mesh cathode placed 5 mm above the grid. The mesh cathode was positively biased and the photocurrent was measured on the grounded anode. From a field strength of around 0.5 kV/cm all of the photoelectrons are extracted and the extraction level becomes almost constant.

Gain measurement in current mode

The detector is used in multiplication mode by biasing the grid negatively, the mesh cathode is biased at the same voltage and the anode is grounded. The current can be measured on the grounded anode. The gain of the detector is defined as the ratio of the anode current with the anode current plateau level, at low gain, before the offset of gain. Figure 5.5 shows various gain curves for different gas mixtures. The best results, best exponential behavior and highest stable gain, is achieved with Ar/CH_4 (95/5). In pure Ne the detector gain is quickly unstable; (photon) feedback effects lead to very high gain levels at low voltage bias. By adding methane as a quencher to the neon the behavior becomes better, but not as good as the result with Ar/CH_4.

Transmissive and reflective photocathodes

Instead of using a reflective photocathode that is deposited on the grid surface the detector can also be combined with other cathodes such as a transmissive photocathode that is part of a window above the detector. The difference is illustrated in

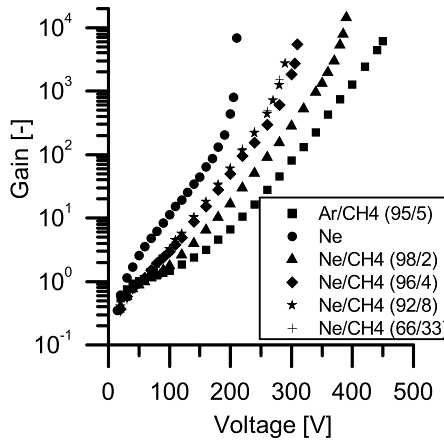

***Figure 5.5** – Gain curves of a single anode device obtained in different gas mixtures as indicated. Gain is determined from current mode measurement, with the assumption that gain = 1 at the low bias plateau.*

fig. 5.6. The transmissive photocathode is a thin layer of CsI, typically 10–20 nm, deposited on a quartz window. The CsI layer has a high sheet resistance, to improve the biasing of the cathode a 10 nm thin layer of Cr is first deposited on the window. This layer stack is semi-transparent, the CsI side of the window faces the detector. Light falls through the window and photoelectrons are emitted into the gas layer beneath the window, this space between the window and the grid is called the drift region. An electric field is applied in this region so that electrons drift towards the grid. Subsequent multiplication is the same as in the case of a reflective photocathode.

In one experiment a single InGrid detector is first used with a separate semi-transparent photocathode and after that a reflective photocathode is deposited and the detector gain is measured again. The detector had holes of 29 μm at a pitch of 58 μm, the amplification gap was 80 μm. Figure 5.7 shows gain curves of this detector measured in Ar/CH_4 (95/5). The reflective mode operation was achieved in the same way as before. For transmissive mode operation the cathode surface is grounded, the grid is kept at a fixed positive bias and the anode is also biased positively with a varying voltage. The grid voltage was 280 V, the grid-to-cathode distance was 5.6 mm, the drift field strength is therefore 0.5 kV/cm. In a separate measurement to characterize the photocathode it was determined that at this field strength a photocurrent of 0.189 nA is extracted. The gain in transmissive mode is calculated by dividing the measured current with the extraction level. The gain therefore includes the efficiency of transfer and collection of primary electrons

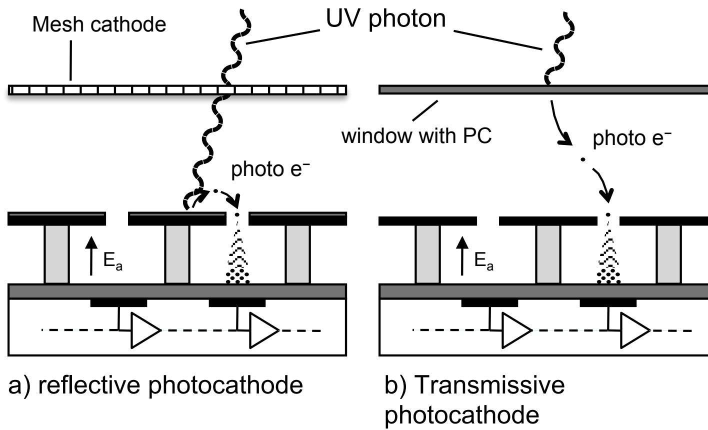

Figure 5.6 *– Operation principles with two different types of photocathode. a) Shows the use of a reflective photocathode deposited on the grid surface, the electric field above the grid is optimized for collection and transfer of primary electrons towards the grid holes. b) Shows a transmissive photocathode deposited on a separate quartz window, the electrons emitted at the underside of the cathode drift towards the grid following the drift field. This mode of operation is similar to that used by other gaseous detectors where electrons are created in the drift region by interactions of particles with the gas.*

through the drift region and into the holes of the grid. The gain curves in fig. 5.7 are almost identical. At low bias voltage, before the onset of multiplication it can be seen that the the collection of the primary electrons from the transmissive photocathode is far from optimal.

Collection of primary current

In reflective mode the collection efficiency can be studied by comparing the extracted photocurrent during photocathode characterization with the current arriving to the anode during multiplication, i.e. during a gain measurement. Figure 5.8 shows these two curves. The horizontal axis shows the electric field. For the photocathode current this is simply the applied electric field strength. In the case of the anode current the curve is plotted against the multiplication field strength scaled with a fit factor. This is not physically correct since, at a given multiplication field strength below the grid, the field above the grid varies over the grid surface according to the distance to the grid holes. For more details on the field distribution see section 4.4. The field scaling does allow easy comparison of the current level, the assumption is that a weighted average ratio between the field above and below the grid can be chosen so that the two curves start to bend upwards at the same lo-

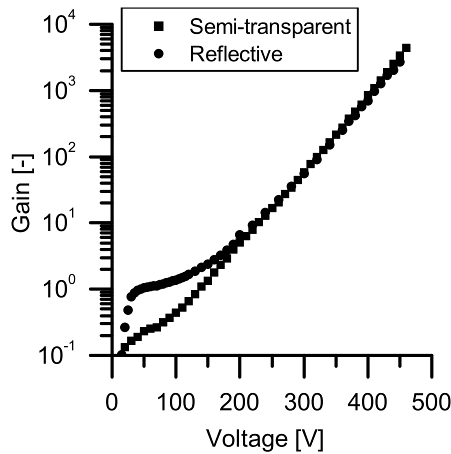

***Figure 5.7** – Two gain curves of a single anode device obtained with a two different types of photocathode. First the device is coupled to a transmissive photocathode, after that the device is removed from the set-up, a reflective photocathode is deposited on the grid and the device is characterized again.*

cation. At these points avalanche multiplication starts to occur, the field strength at which this happen should be equal in both cases. Figure 5.8 shows that all of the cathode current arrives at the anode, before multiplication starts to occur, once sufficient field strength is applied to drift the primary electrons into the grid holes. The collection efficiency of these primary electrons is nearly perfect.

Ion current

In gaseous detectors such as these, ions are created in the multiplication space, the ion current is identical to the electron current that arrives at the anode. Most of these ions arrive to the bottom of the grid. Some of them arrive at the photocathode surface. These ions might have a detrimental impact on the photocathode performance. In the test device with a semi-transparent photocathode all three detector terminals can be connected separately. The photocathode is grounded, this terminal is connected to a precision ammeter. Current from the other terminals can be determined by measuring the voltage drop over a series resistor. It is therefore possible to measure which part of the ion signal arrives to the photocathode. This fraction of the total ion current is known as the Ion Backflow Fraction (IBF). The IBF is calculated by dividing the rise in cathode current with the anode electron current, as shown in eq. 5.1.

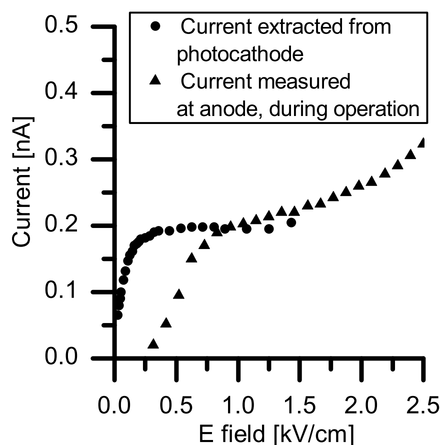

Figure 5.8 – Current contributions, the curve with circular symbols shows the current extracted from the photocathode against the applied field strength, measured during photocathode characterization. The curve with triangular symbols shows the anode current as measured during operation of the detector.

$$\begin{aligned} IBF &= \frac{I_{cathode,ions}}{I_{anode}} \\ &= \frac{\Delta I_{cathode}}{I_{anode}} \\ &= \frac{I_{cathode} - I_{cathode,zerobias}}{I_{anode}} \end{aligned} \tag{5.1}$$

The cathode current at zero bias, before multiplication starts, is the extracted electron current. This level is assumed to be constant for a constant drift field strength. Figure 5.9 shows a plot of the IBF for the device coupled to a transmissive photocathode. At maximum gain (the grid-to-anode bias voltage is 470 V) the $IBF \approx 2\%$.

5.2.2 Pulse measurements

The charge that arrives at the anode after a photoelectron is multiplied can be recorded using an external charge sensitive amplifier connected to the anode electrode. The output of this amplifier (voltage pulses) are further amplified using an Ortec 570 linear amplifier and the pulse height spectra are recorded with am Amptek 8000A Multi Channel Analyzer (MCA). The total voltage pulse height range is divided in bins and a histogram is created for all pulses detected during

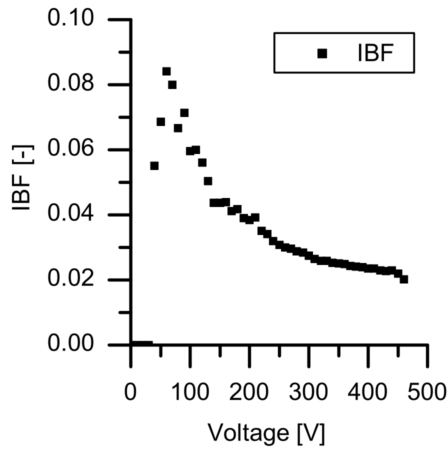

Figure 5.9 – *IBF of the single anode InGrid device coupled to a transmissive photocathode, measured in Ar/CH_4 (95/5). The x-axis indicates voltage applied across the avalanche gap.*

a certain acquisition time. The MCA counts the voltage peaks within a range of charge bins. The procedure is similar to the one for the chip based detectors described in section 4.7.1 except that there the preamplifier is connected to the grid and it is integrated onto the readout PCB and is therefore much closer to the device. This means there is less possibilities for noise and other interferences.

Figure 5.10 shows pulse height spectra for a single anode detector with holes of 13 μm at a pitch of 20 μm and a 50 μm gap height.

The expected curves for single photon detection are sharp triangular shapes (an exponentially decreasing gain distribution) that extends to low count rates. The slope should be lower for higher gain, average gain is defined by the integral of the pulse height spectrum divided by the total amount of pulses for a large set of events. The curves in fig. 5.10 seem to have a relatively constant slope. The distribution is also noisy, especially for the lower bias values. These curves have been corrected for dark noise (which is a single high peak at low charge). In addition there is a noise contribution from feedback effects. This shows up as the large contribution of pulses with a high charge and a relatively low count rate. The single photon pulses cannot clearly be separated.

It is evident that the readout method used here is not adequate. This device with a single unpatterned anode is very large. It has a very large capacitance that makes it difficult to record very small charge pulses. Furthermore the pre-amplifier is relatively far away which means that lossy and noisy long cables are needed. In further experiments the InGrid devices are coupled to Timepix readout element.

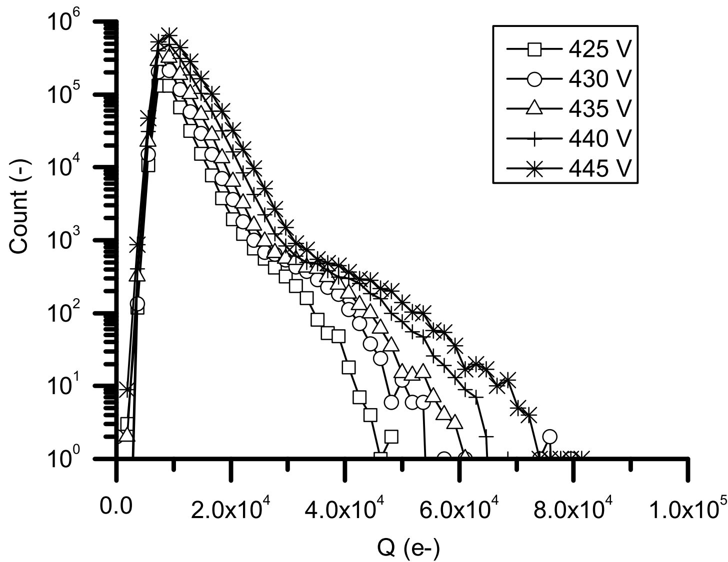

Figure 5.10 *– Pulse height spectra of the single anode InGrid device with varying grid bias. The horizontal axis is calibrated in units of e^- charge. The acquisition time was 100 s.*

The superior readout of these imaging chips allows much better detection of very small signals.

5.3 Results with chip based detectors

In a second set of experiments the InGrid detectors are combined with Timepix readout chips. The following sections document various results obtained. Current mode measurements with this arrangement are not possible: the chip surface has to be grounded and the current to this composite terminal cannot be measured externally.

It is possible to measure pulse signals on the grid, for this purpose a charge sensitive preamplifier is included on the readout PCB. This preamplifier is connected to the grid electrode. The preamplifier also has an external input for calibration. using a voltage pulse generator and a capacitor a known charge can be injected into the amplifier. The charge sensitive preamplifier outputs voltage pulses, these are then further conditioned using timing and shaping amplifiers. The voltage pulses are finally analyzed by a Multi Channel Analyzer (MCA) to take pulse height spectra.

Finally measurements can be made using the pixel readout of the chip. With these imaging experiments can be made.

5.3.1 Gain as determined from pulse measurements

The gain of the detector was determined using two different methods. In the first experiment ^{55}Fe is used as a radiation source, the emitted 5.9 keV photons convert in the gas volume. They collide with gas atoms, this leads to the emission of a number of primary electrons. The charge that is created drifts towards the grid and is then multiplied by the detector. In the He based gas mixture that was used the primary charge cloud consists of on average 160 electrons. The second method uses irradiation with UV light. Photons convert on the photocathode surface and the primary electrons enter the grid holes and are then multiplied and detected. The light flux is reduced by placing the light source far away from the detector and illuminating through a pinhole aperture. The light is further reduced by placing semi-transparent absorbers in the beam path. The reduction is sufficient to reach a situation where the pulses of individual photons can be discriminated by the amplifier chain. In this case the pulses are initiated by single primary electrons.

In both cases the charge pulses on the grid are recorded using a charge sensitive amplifier that is calibrated before hand by injecting known charges with a capacitor and a voltage pulse generator. The procedure is described in section 4.7.1. The grid and the cathode mesh are biased with negative high voltage potentials, the anode is grounded. For the ^{55}Fe measurements the cathode mesh is biased at a 100 V higher voltage than the grid. The distance between grid and the cathode mesh was 2.2 mm, there is therefore a constant drift field of approximately 0.5 kV/cm. This field strength is high enough to allow good collection of primary charge and at the same time low enough to prevent avalanche gain in the drift region. For the measurements made with UV light irradiation the cathode mesh and grid electrode are biased at the same voltage as is usual for photon detection. All measurements presented here were done in He/iC_4H_{10} (80/20) at atmospheric pressure.

Measurements using an ^{55}Fe source

The gain is determined before and after the CsI photocathode is deposited. With ^{55}Fe irradiation the signal does not require the photocathode. To prevent any influence of ambient light the experiments are carried out in the dark. The measured pulse distributions have also been corrected for noise. For this purpose separate noise distributions have been recorded for each bias condition.

The measured gain curves are plotted in fig. 5.11. The lines are almost parallel. The bare device, before CsI deposition, has a characteristic slope of 98.2 ± 2.6 V/decade. After deposition of the CsI photocathode the same device gives a gain to bias dependance of 99.2 ± 1.4 V/decade. The curves have different abso-

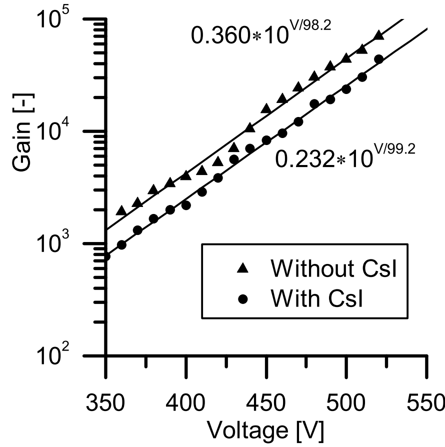

Figure 5.11 *– Gain before and after deposition of the CsI photocathodes. The symbols are measured data, obtained in He/iC_4H_{10} (80/20). The drawn lines, and the accompanying formulas, are fitted to the measured data.*

lute gain level, the fitted gain of the CsI coated device has a prefactor that amounts to 64% of that of the bare device. This difference is most likely explained by a difference in irradiation conditions by the ^{55}Fe source. In both cases the curves are exponential up till a grid bias voltage of 520 V. There is no evidence of enhanced secondary effects such as photon feedback after the introduction of CsI.

Measurements using UV light

The same detector as was used for the ^{55}Fe has also been used for a determination of the response to single photons.[2] Pulses were recorded from the grid. The exponential pulse-height spectra (typical for single-photon gas avalanche detectors) for a range of bias voltages are shown in fig. 5.12. The distributions are accurately described by eq. 5.2, where N is the amount of hits, Q is charge, G is the average gain and C is a constant.

$$N(Q) = C \cdot 1/G \cdot \exp(-Q/G) \qquad (5.2)$$

By making fits to the measured spectra we determined average gain G for all voltages. The results of this gain determination has been plotted in fig. 5.13. In the same graph also the gain curve determined with ^{55}Fe is plotted. The gain levels are not equal. This can be due to a different in the way the absolute gain is calculated. For instance in the case of the ^{55}Fe measurement a certain yield of primary electrons (around 160) is assumed upon interaction with the He ambient.

[2]From an Ar(Hg) lamp, see section 4.7.

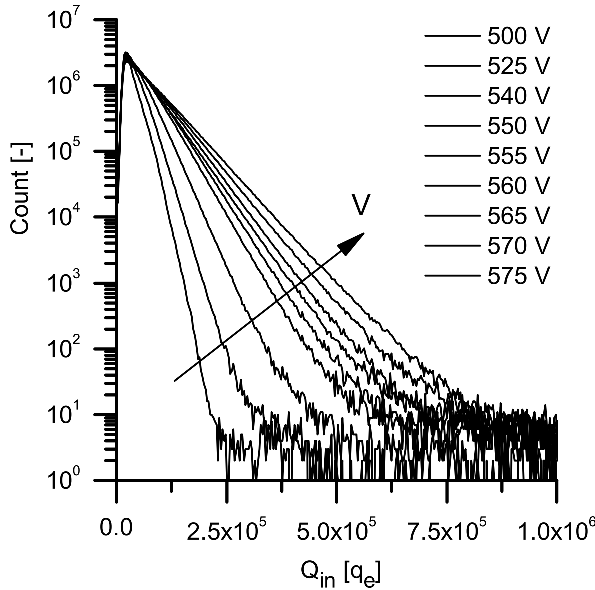

Figure 5.12 – *Pulse-height spectra for a range of bias voltages, recorded on the grid under UV irradiation.*

Not all of this charge may reach the grid holes. The emitted x-ray photons from the source reach the gas volume through a Kapton window on the side, next to the UV transparent quartz window. This requires that the beam enters with a very shallow angle, this leads to inaccuracies in the conversion and collection of the primary charge. Curves are fitted to the gain data, the prefactors of these curves are compared and using these the ^{55}Fe data is shifted so that the curves are equalized. There is good agreement between the two methods; with ^{55}Fe we obtained a slope of 100.0 V/decade and with UV photons it is 111.1 V/decade. The maximum gain that was reached is $6 \cdot 10^4$.

5.3.2 Spectra with and without CsI

To investigate the influence of CsI coating on the device performance a test has been made with partial CsI coating. A chip with post-processed InGrid is loaded into the evaporation chamber with a shadow mask placed close to the chip in such a way that most of the chip will be coated but the bottom quarter of the pixel array remains bare. Figure 5.14 shows an image of the chip readout over the whole array, the coated region on top shows much higher output (red) than the bottom quarter (mostly blue). Different regions can be tested separately by illuminating them individually using a mask with a small hole in it. Area A is in the uncoated area,

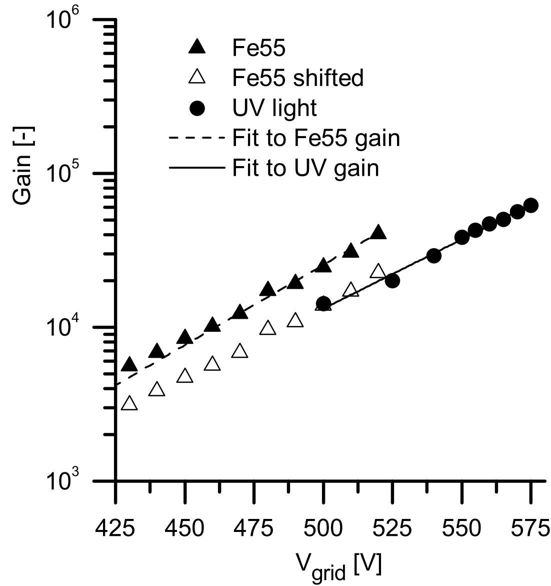

Figure 5.13 *– Gain curves of the same device obtained with ^{55}Fe and with UV radiation. Exponential fits are made to the data, using the difference in prefactors the ^{55}Fe data is shifted and replotted for comparison.*

the spectrum measured in this zone is given in fig. 5.15. Area B is diametrically opposite of the array, a spectrum is given in the same graph. This spectrum has a steeper slope, indicating that the local gain is lower (see eq. (5.2)). The gain difference is caused by a different local gap height, it is thought that the proximity of the edge changes the SU-8 pillar height (due to the lithographic process) or deformation of the Al grid. The gap height in area B is different from area A, despite being at the same distance to the edge of the imaging array, because of the presence of the section of the chip reserved for bondpads and peripheral electronics located below area A. Area C is more similar, being farther from the edge (than B), the slope (and gain) are similar to area A. The spectrum is also graphed in fig. 5.15. A comparison of the spectra from areas A and C, without and with CsI, we do not see a difference other than the lower level of the spectrum for A, owing to the lower quantum efficiency of the non coated region. Feedback effects, that could be enhanced by the addition of CsI, would show up as an enhanced contribution of counts with a high charge, in the tail of the spectrum.

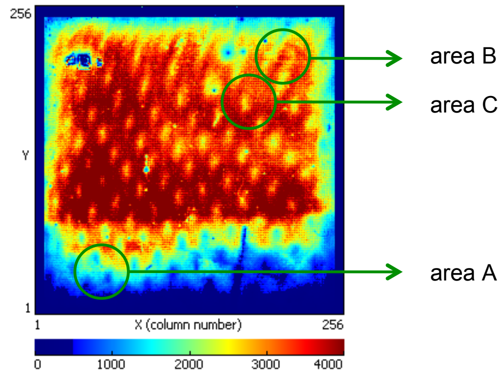

Figure 5.14 *– Frame with TOT count showing the higher signal (the red region) coming from the area where the CsI is deposited, the blue region in the bottom part of the chip is not coated with CsI, as a result of this it generates much less signal.*

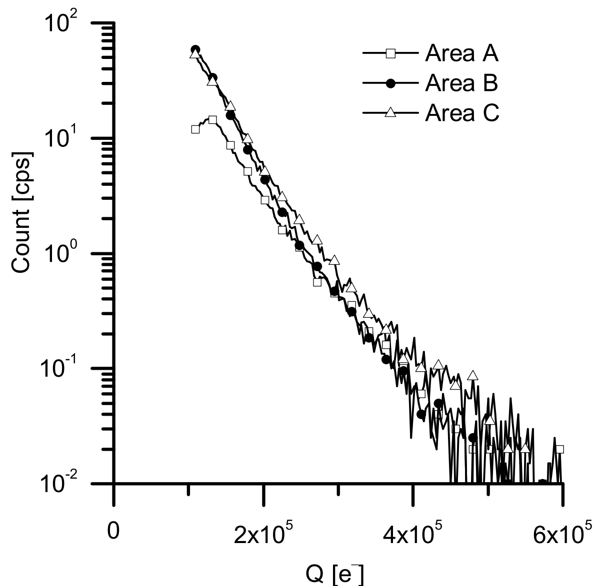

Figure 5.15 *– Spectra of the three different areas of the detector, area A is uncoated and the other regions (B and C) are coated with CsI. The spectra are given in counts/second.*

5.3.3 Using the TOT count to establish bias dependencies

The Timepix chip can be read out in different ways. One of these ways is to measure the time that the input signal on each pixel remains above a predetermined threshold, this metric is called the Time Over Threshold (TOT) count. There is a global threshold level that can be set by the user. The threshold level can be adjusted individually for each pixel to account for sensitivity variations across the matrix. A calibration procedure is performed for each chip and the resulting matrix of threshold adjustments is stored and used each time the data is read out.

When charge is deposited onto a pixel pad it is drained at a fixed rate, determined by the current that enters the charge sensitive amplifier. The TOT count is therefore, within certain limits, linearly dependent on the deposited charge. The TOT count can be used to make charge measurements.

Gain measurement using the TOT count

In one experiment the gain in the central region of a CsI coated device is determined by plotting the total TOT count of all pixels in that area, during a certain time. For this experiment the area was the central square of 100×100 pixels. The TOT count is plotted against the grid bias voltage in fig. 5.16 together with the UV gain determined before (in section 5.3.1). For both gain curves exponential fits are made. The slopes are comparable. For comparison the TOT data is replotted after shifting it downwards with a factor equal to the ration of the fit prefactors.

Cathode bias dependency

In most experiments the cathode mesh is biased at the same voltage as the grid. To investigate the influence of the bias voltage the TOT count is measured under UV illumination with a varying voltage applied to the cathode mesh. The bias voltage of the grid was always 500 V, corresponding to a field strength of 62.5 kV/cm (gain $\approx 1.2 \cdot 10^4$). For this measurement 4 frames are measured consecutively and the sum TOT count of the entire frame is averaged and divided by the collection time (20 s) to give a count-rate. This metric is used to evaluate the performance of the device, this indicator depends both on the extraction efficiency as well as the collection efficiency of primary charges. If a higher negative potential is applied to the mesh cathode (than to the grid) the electric field in the drift region is positive, this suppresses the extraction of photoelectrons from the grid, electrons are pushed back into the photocathode. If the field is reversed (so the bias to the mesh cathode is lower, closer to ground, than that of the grid) the collection is suppressed, electrons are attracted towards the mesh cathode and do not reach the grid holes. Figure 5.17 shows the measurement results, for this specific device an optimum is found with around 1 kV/cm drift field.

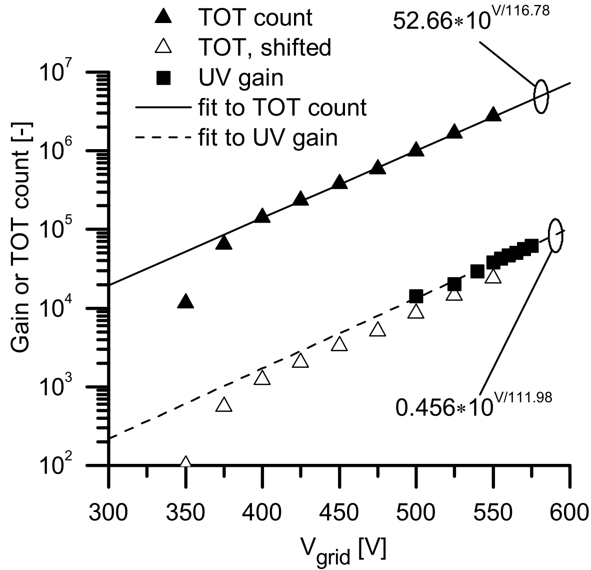

Figure 5.16 *– TOT count of the central part of a Timepix/InGrid device (of* 100×100 *pixels), as well as gain determined with pulse measurements from UV light irradiation.*

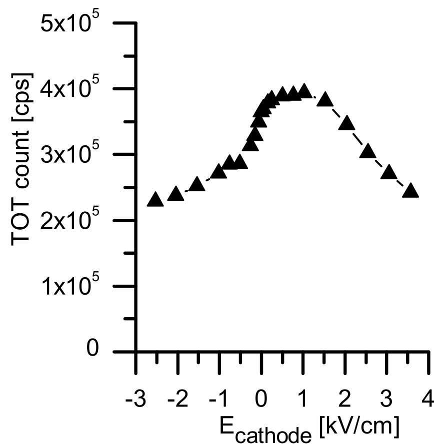

Figure 5.17 *– Average TOT count, expressed in counts/second, against drift field strength.*

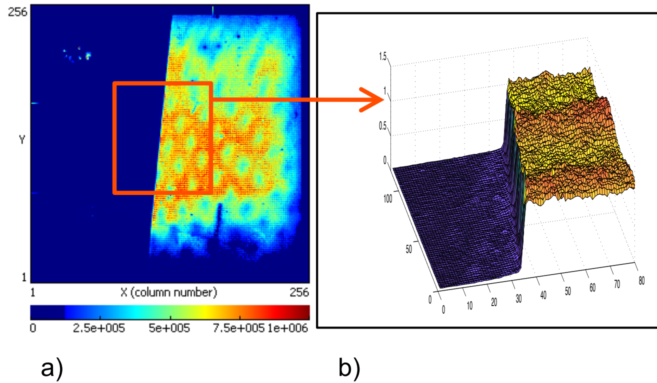

Figure 5.18 – a) An image of a slanted metal sheet, the data of a certain ROI is considered, the raw image data is corrected with an open frame measurement taken under the same conditions providing the step response on the right (b).

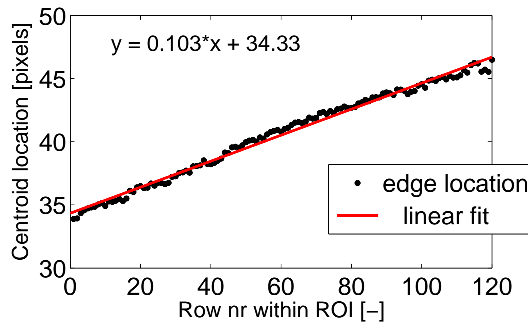

Figure 5.19 – Fit through centroid locations to model the edge step response.

5.3.4 Spatial resolution using the slanted edge method

To determine the spatial resolution we followed the ISO 12233 procedure [123]. Images were recorded under UV irradiation of the edge of a thin sheet of steel placed at a slight angle with respect to the pixel orientation. The response was corrected for fixed patterns by division with data of an open frame (flat field) measurement taken under the same conditions. The step response was analyzed within a certain Region Of Interest (ROI), as shown in fig. 5.18a. For each line of pixels we took the derivative of the pixel counter value and determined the centroid; this defines the edge location within each line of pixels. A linear fit was performed through the centroid locations to derive a description of the edge, this fit is shown in fig. 5.19.

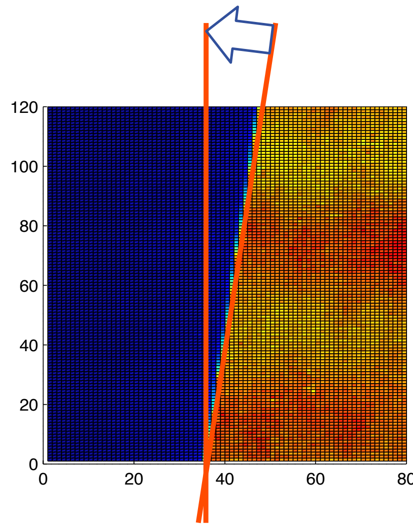

Figure 5.20 – The data of each lines can be shifted according to the fitted edge location, so that all edge locations fall on top of each other.

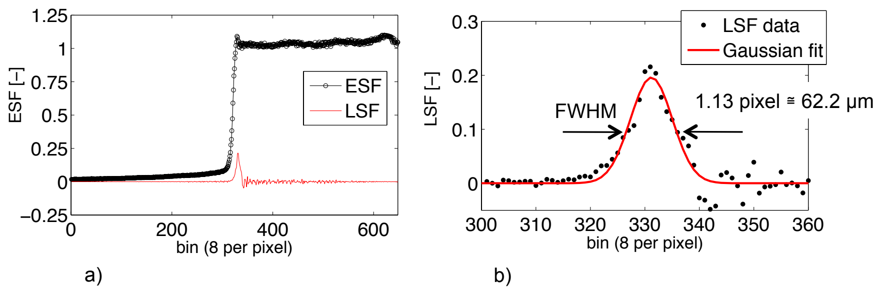

Figure 5.21 – a) ESF as derived from the rebinned data within the ROI, b) LSF data and Gaussian fit.

The pixel data in the ROI is then shifted, line by line, over a distance derived from the fitted edge location. The result is that the edge step in each line is then placed on the same lateral position. This redistribution is illustrated in fig. 5.20. The data of the entire ROI can then be rebinned (in this case with 8 bins per pixel) and added up to create a single Edge Step Function (ESF). The derivative of the ESF is the Line Spread Function (LSF). A Gaussian curve was fitted to the LSF; the 1σ spread is 0.48 pixels or 26.4 μm and the FWHM is 1.13 pixels or 62.2 μm. The results are shown in fig. 5.21.

By performing a Fourier transform of the LSF we obtained the Modulation

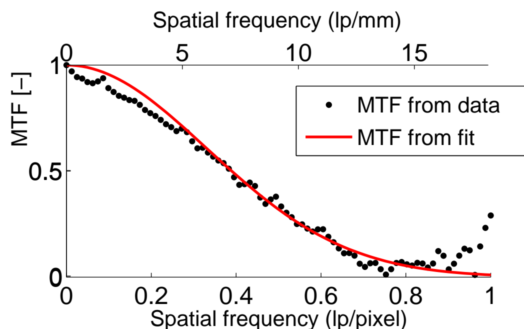

Figure 5.22 – *MTF plot obtained from a Fourier transform of the LSF.*

Transfer Function (MTF) of the entire system. The MTF reaches 50% at a frequency of 0.4 lp/pixels ($\simeq$ 7 lp/mm). The resolution limit is below the pixel pitch, at the Nyquist frequency MTF = 0.32. The resolution limit is reached at 0.8 lp/pixels ($\simeq$ 14 lp/mm). The MTF plot is given in fig. 5.22.

5.3.5 Imaging results

The cathode mesh shown in fig. 4.11, needed to shape the field above the grid, modulates the light reaching the photocathode. In fig. 5.23a we see a Moiré pattern which is the result of using a cathode mesh with a wire pitch of 56 μm and a detector pitch (both grid and read-out pads) of 55 μm. Using a coarser mesh, with a pitch of 500 μm, the mesh wires are directly imaged by the detector (fig. 5.23b). The high resolution permits observing mesh defects. On the left edge we see one of the wires (the eighth wire from the top of the frame) is displaced, probably due to mishandling during mounting of the mesh.

The images in fig. 5.23 were taken with a partial CsI coating. For experimental reasons not discussed here the bottom 15% of the matrix was not coated with CsI, which naturally resulted in a lower response in that region.

5.4 Conclusions

We have presented a monolithic gaseous UV-photon imaging detector with a CsI photocathode. The photocathode deposition and its operation are found to be adequate in combination with both the Micromegas single anode multiplier as well as the imaging chip. Most experiments have been performed in He/iC_4H_{10} (80/20), in which the extraction efficiency is around 50%. The maximum gain that was reached is $6 \cdot 10^4$.

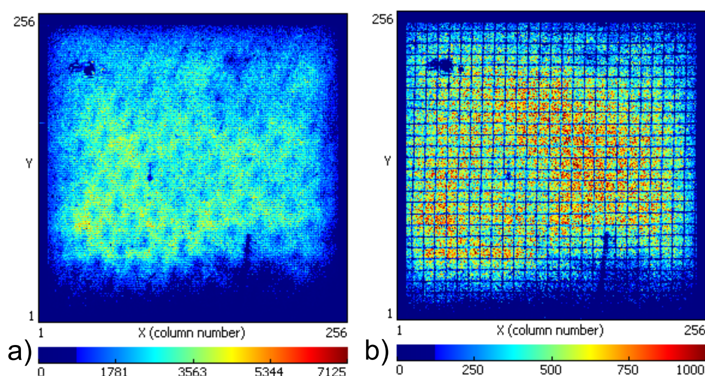

Figure 5.23 – *2D images of flat-field UV irradiation of the detector shown in fig. 4.11 using He/iC_4H_{10} (80/20) at 1 atm. a) Moiré pattern resulting from using a 56 μm mesh above the 55 μm pitch detector and b) direct imaging of the mesh when the mesh pitch is increased to 500 μm.*

Imaging experiments indicate good spatial resolution, the LSF has a spread of 26.4 μm, MTF50 is reached at 0.4 lp/pixel ($\simeq$ 7 lp/mm). The high spatial resolution results from the high level of integration. The technology used to make the detector allows fine dimensional control, also the alignment between grid and readout matrix is near perfect (on the size scale of the pixel pitch). The choice for an integrated reflective photocathode, placed directly onto the grid, limits lateral diffusion of primary charge which would deteriorate the spatial resolution.

Many high quality 2D images were recorded. These also show the good resolution, for instance in the case where a very coarse cathode mesh is used. This mesh is perfectly imaged, including its defects.

These encouraging results suggest further investigations directed towards the search for operation conditions and gas-mixtures assuring better photoelectron collection efficiencies (lower backscattering). Investigations of absolute photon detection efficiencies and of ion-blocking (ion-feedback) are required. The new device could find applications in high-resolution imaging of UV photons. Furthermore, being made of UHV-compatible materials, it could be applicable as a multiplication and readout element also in cascaded visible-light imaging gas photomultipliers [122].

Chapter 6

Towards integrated MCPs

The previous chapters have dealt with gaseous detectors. Other detector types have also been considered, specifically detectors that operate in vacuum. One common element used for electron multiplication is a Micro Channel Plate (MCP). These are plates of a non-conductive material with long vertical pores that extend the full thickness. MCPs can be coupled both to reflective as well as transmissive photo-cathodes, similar to gaseous detectors. The readout of the amplified charge signal is also similar to that for gaseous detectors. Vallerga *et al.* have used Medipix2 [33] and Timepix [35] chips to record the signals of MCPs. The MCPs were mounted above the anode plane using mechanical fixtures. In line with the aim of making a monolithic post-processed detector we have investigated the possibility to manufacture an MCP structure directly onto CMOS imaging chips. Two different approaches have been taken, one is to make the pore structure out of anodized aluminum, the other is to fabricate a high aspect-ratio SU-8 pore structure. The anodized aluminum material will be called Porous Anodic Alumina (PAA).

6.1 MCP principle of operation

For a general description and an illustration of the MCP operation principle we refer to section 1.1.2 and fig. 1.5. The primary signal, this could be a single photo-electron, enters a pore at the top surface. Due to the applied field it is accelerated. MCPs multiply electron charge signals by successive collisions with the sidewall. At each collision more charge carriers are generated. The process is similar to that of a Photo Multiplier Tube (PMT), except that there are no discrete dynodes. The sidewalls of the pores can be regarded as one distributed dynode. To power the multiplication process and to provide the drift field for the electrons a bias voltage is applied across the MCP. For this purpose the faces of the MCP are typically coated with a conducting material. The MCP structure itself is normally a dielec-

tric material. The sidewalls of the pores are coated with a layer that enhances the creation of secondary electrons. At the other end of the pore the multiplied charge exits the structure, it can then be collected by a readout array such as Timepix.

Conventional MCPs are made out of bundles of glass tubes that are drawn out to create a high aspect-ratio. The techniques are similar to those used for optical fibers. Disks are cut out of the bundles and the cores are etched away to create open structures. Typical pore sizes are in the range 5–15 μm, the pore length (the thickness of the disks) is between 200 and 1000 μm. Post-processed MCPs, made with MEMS technologies, have much smaller geometries. Pore lengths cannot be more than 100 μm, this implies pore diameters in the range 0.5–1 μm. References [124, 125] present another alternative method to manufacture MCPs using micro-machining technology. A porous structure is created by dry etching of a monosilicon Si substrate. The Si matrix is then converted to a dielectric siliconoxide MCP by thermal oxidation of the complete substrate [124, 125].

One interesting development is reported in [126] by Tremsin and coworkers. ALD (Atomic Layer Deposition) techniques are used to deposit layers over the entire channel wall. ALD allows to deposit all the way to the bottom of very deep porous structures. The layer deposition provides the opportunity to tune the sidewall resistivity and the secondary electron yield. With this low temperature technique it seems possible to manufacture MCPs out of non-traditional materials such as plastics. The authors claim the process temperature is below 150 °C.

6.1.1 Gain model and simulation results

The following gain model is well known from literature [28, 127], it is used here to investigate the operation of MCPs with small holes. The total gain, G, of each of the pores is defined by the number of collisions, n, and the amount of secondary electrons created at each collision, δ. This last metric varies with the acceleration voltage the carriers experience between two collision steps, V_{coll}, and a material dependent constant, A, expressed in $\text{V}^{-0.5}$. The number of collisions n is related to the total length L of the pore and the length l_{coll} between collisions, n also defines the ratio between the energy step V_{coll} per collision and total applied voltage V. The relations are given in eq. (6.1). An illustration is given in fig. 6.1.

$$\begin{aligned} G &= \delta^n \\ \delta &= A \cdot \sqrt{V_{\text{coll}}} \\ n &= \frac{L}{l_{\text{coll}}} \\ V_{\text{coll}} &= \frac{V}{n} \end{aligned} \tag{6.1}$$

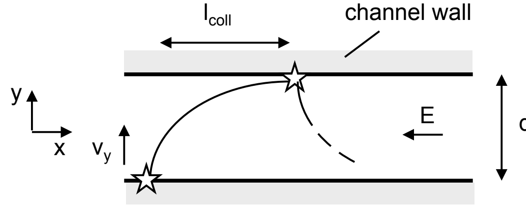

Figure 6.1 *– Collision process inside one channel of an MCP. Electrons collide between opposite sides of the pore sidewall. While crossing the pore diameter d they drift down the pore driven by field E.*

All secondary electrons are assumed to leave the sidewall perpendicularly with an energy $q \cdot V_0$. This defines the kinetic energy and therefore their speed v_y with which the electrons traverse the pore width and thereby the time t_{coll} it will take before the next collision (on the opposite side of the pore). This time t_{coll} is needed to calculate how far along in the x-direction the electrons will travel in each step. The time t_{coll} is calculated in eq. (6.2), q is the elementary electron charge and m is the electron mass.

$$\begin{aligned} E_y &= \frac{1}{2} \cdot m \cdot v_y^2 = V_0 \cdot q \\ t_{coll} &= \frac{d}{v_y} \rightarrow t_{coll} = \frac{d}{\sqrt{\frac{2 \cdot V_{coll} \cdot q}{m}}} \rightarrow t_{coll}^2 = \frac{d^2 \cdot m}{2 \cdot V_{coll} \cdot q} \end{aligned} \tag{6.2}$$

Along the length of the pore, in the x-direction, the secondary electrons start with zero speed, they are accelerated by the field V/L, if we integrate this acceleration a_x twice over time t we can find the distance l_{coll} until the next collision (at the opposite side).

$$l_{coll} = \frac{1}{2} \cdot a_x \cdot t_{coll}^2 \tag{6.3}$$

The electrons are attracted by the electric field, this leads to eq. (6.4) for the acceleration, where F is the drift force acting on the electron.

$$\begin{aligned} F = m \cdot a_x \text{ and } F = E \cdot q = \frac{V}{L} \cdot q \\ a_x = \frac{V \cdot q}{L \cdot m} \rightarrow l_{coll} = \frac{V \cdot q}{2 \cdot L \cdot m} \cdot t_{coll}^2 \end{aligned} \tag{6.4}$$

Combining the two sets of equations, in the x- and the y-direction, that define t_{coll} we find the following expression for n eq. (6.5). The aspect ratio of the pores, α, is defined as L/d.

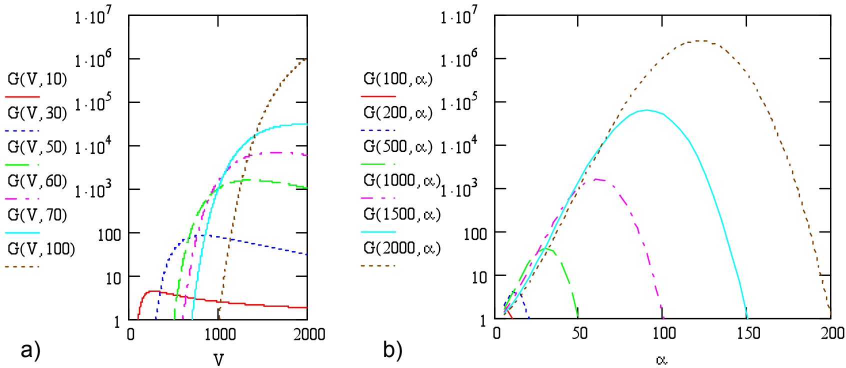

Figure 6.2 *– Gain as a function of bias voltage and aspect ratio, $G(V, \alpha)$, for a) a range of α and b) a range of V.*

$$
\begin{aligned}
l_{\text{coll}} &= \frac{V \cdot q}{2 \cdot L \cdot m} \cdot t_{\text{coll}}^2 = \frac{V \cdot q}{2 \cdot L \cdot m} \cdot \frac{d^2 \cdot m}{2 \cdot V_0 \cdot q} = \frac{V \cdot d^2}{4 \cdot L \cdot V_0} \\
n &= \frac{L}{l_{\text{coll}}} = \frac{L \cdot 4 \cdot L \cdot V_0}{V \cdot d^2} = \frac{4 \cdot V_0 \cdot \alpha^2}{V}
\end{aligned}
\tag{6.5}
$$

These expressions can then be entered into eq. (6.1) to yield eq. (6.6).

$$
\begin{aligned}
\delta &= A \cdot \sqrt{V_{\text{coll}}} = A \cdot \sqrt{\frac{V}{n}} = \frac{A \cdot V}{2 \cdot \alpha \cdot \sqrt{V_0}} \\
G &= \delta^n = \frac{A \cdot V}{2 \cdot \alpha \cdot \sqrt{V_0}}^{\frac{4 \cdot V_0 \cdot \alpha^2}{V}}
\end{aligned}
\tag{6.6}
$$

The only remaining geometry factor in eq. (6.6) is the aspect ratio (α). This suggest that the MCP can be scaled. For fig. 6.2 the model described above is used to plot the dependence of G on V and α. We assume $A = 0.2$ and $q \cdot V_0 = 1$ eV [28].

6.1.2 Choice of the geometry

Figure 6.2 clearly shows that although the geometry can be scaled arbitrarily the required voltage to reach a certain gain does not change significantly. This can be understood if we imagine that the energy required to extract a certain number of charge carriers (related to the gain) does not change when the structure is made

smaller. This energy ($\propto q \cdot V^2$) is supplied by the bias voltage. If the Timepix readout is used a gain of 1000–2000 is needed. This means a voltage of at least 1000–1500 V is required. This puts certain demands on the dielectric strength of the material that is used. The aspect ratio needs to be in the range 50–100, this is similar to conventional MCPs. If the pores are too long relative to the diameter (high α) there are too many collisions with only a limited voltage drop per step, this means the electrons do not gain enough energy to create (several) secondary electrons. If the pores are too short relative to the diameter (low α) there will be too little collisions, the electrons travel too far down the pore during the time it takes them to traverse the width of the pore.

Another consideration is gain saturation, this will limit the minimal pore width. If a too high concentration of carriers develops at the bottom end of the pores the charge repulsion will smother further multiplication, leading to saturation of the gain/diameter ratio, a typical limit is 10^5 -/μm [28]. This indicates that a true Nano-Channel Plate would not work, for a typical gain requirement of 10^3 a minimal diameter of 10 nm is needed.

The minimum pore width is determined by two factors. The minimum layer thickness (given the dielectric strength and the required bias voltage of 1000 V) and the patterning technique. For the PAA structure the pore sizes can be in the range 0.1–0.5 μm, the pore pitch is 0.5–1 μm. PAA typically has a hexagonal packing structure. Experimental results are given in section 6.2. SU-8 structures are envisaged to be have a pore size of 1–2 μm and a pitch of 2–4μm.

Bias current and pore size

The pore density depends on the pore pitch and the ordering, if we assume a pore pitch p and hexagonal packing the density of pores, ρ_{pores}, is given by eq. (6.7).

$$\rho_{\text{pores}} = \frac{1}{A_{\text{pore}}} = \frac{1}{\frac{1}{2} \cdot \sqrt{3} \cdot p^2} \approx \frac{1.15}{p^2} \tag{6.7}$$

Each pore has a resistance related to its geometry and the sheet resistance of the pore surface, $R_\square$. A value of $10^{13}\Omega$/sq is typical for dielectric materials, this is also a common value for the material used for MCPs. The resistance from top to bottom is given by eq. (6.8). If we assume the pore to have an aspect ratio of 50 the pore resistance becomes $1.59 \cdot 10^{14}$ Ω.

$$R_{\text{pore}} = R_\square \cdot \frac{L}{\pi \cdot d} = R_\square \cdot \frac{\alpha}{\pi} \tag{6.8}$$

Combining eq. (6.7) and eq. (6.8) we obtain an expression for the specific resistance R_{spec} for the MCP, as shown in eq. (6.9).

Table 6.1 – MCP geometry and the effect on strip current per pixel for a Timepix pixel.

geometry	pitch [μm]	ρ_{pores} [-/cm^2]	R_{pore} [Ω]	R_{spec} [Ω/cm^2]	I_{pixel} [nA]
PAA min	0.5	$4.62 \cdot 10^8$	$1.59 \cdot 10^{14}$	$3.45 \cdot 10^5$	87.8
PAA max	1	$1.15 \cdot 10^8$	$1.59 \cdot 10^{14}$	$1.38 \cdot 10^6$	21.9
SU-8 min	2	$2.89 \cdot 10^7$	$1.59 \cdot 10^{14}$	$5.51 \cdot 10^6$	5.5
SU-8 max	4	$7.22 \cdot 10^6$	$1.59 \cdot 10^{14}$	$2.21 \cdot 10^7$	1.4

$$\begin{aligned} R_{\text{spec}} &= \frac{R_{\text{pore}}}{\rho_{\text{pores}}} = R_{\square} \cdot \frac{\alpha}{\pi} \cdot \frac{1}{2} \cdot \sqrt{3} \cdot p^2 \\ &\approx 0.276 \cdot R_{\square} \cdot \alpha \cdot p^2 \end{aligned} \tag{6.9}$$

Given the specific resistance and the bias voltage we can then find the leakage current through the MCP, this current is known as the strip current. If the MCP is integrated directly onto a Timepix readout this current will have to be drained by the pixel input. The pixels have a size of $55 \times 55 \mu\text{m}^2$. The pore density, specific resistance and leakage current (per Timepix pixel) are given in table 6.1 for four different cases. For the two materials that are considered, PAA and SU-8, the results are given for a minimum and maximum sized pore. For PAA the minimum size given is the maximal pore size found in literature [128], around 500 nm.

The preamplifiers in each Timepix pixel contain a differential amplifier. They can drain a current of maximally half of the tail current that is used [63]. The default tail current is 14 nA, in which case the PAA based MCPs are not feasible with the assumptions made above. The tail current can however be increased, at the price of sensitivity. Still it is advisable to make the pore pitch as large as possible. Attempts at that are discussed further in section 6.2.

Dielectric strength and thickness

In chapter 2 it is determined that the dielectric strength of SU-8 is 440 V/μm. With a pore size of 1–2 μm the SU-8 MCPs will have a thickness of at least 50–100 μm, assuming a minimum aspect ratio of 50. This means the MCPs can be biased with at least 2–4 kV, this allows ample room for the operation of an MCP. PAA MCPs are thinner, 5–25 μm. The dielectric strength is difficult to determine. An initial test with 50 μm PAA disks showed no problems up to a bias voltage of 2000 V. A higher test voltage was not available in the measurement setup that was used. Literature reports on the dielectric strength of PAA

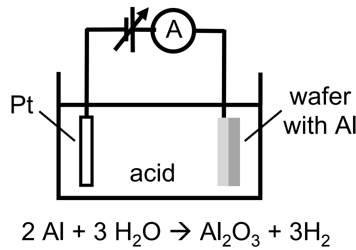

***Figure 6.3** – Anodization process, the acid in the bath is typically sulfuric, oxalic or phosphoric acid.*

give diverse results, but it appears to be at least 100 V/μm [129]. If this is true the thickness should be at least 10 μm, however the real dielectric strength is most likely higher than the quoted value, given the results for SU-8.

6.2 Al_2O_3 MCP structures

The MCP is made out of porous alumina. This layer is made by anodically oxidizing a thick layer of Al placed over the Al bondpads of the Timepix chip. The process is completely IC compatible. On top of the IC wafer a thin counter-electrode and a thick pure Al layer are deposited by sputtering. The wafers are immersed in an acidic solution and a bias is applied between the metal stack and a Pt anodization electrode. The Al is converted into a self-organized porous Al_2O_3 structure, the process is illustrated in fig. 6.3. Non-integrated PAA MCPs have been proposed by researchers from Belarus [130, 131]. Whikun *et al.* have presented a low aspect-ratio alumina capillary structure for charge multiplication. These structures were made by stacking layers of perforated bulk alumina films [132, 133].

The main instrument to control pore width and pore pitch is the anodization voltage [134]. Typical ratios of pore width and pitch to voltage are around 2–4 nm/V. More results can also be found in the papers by Masuda *et al.* [135, 136, 137, 138] and Li *et al.* [139, 140, 128]. PAA formation has previously been used to make photonic crystals, with pore sizes of close to 0.5 μm [139, 138], this is within the useful range for MCPs.

Several experiments with Al anodization have been performed on samples with thick Al layers. Typical results of SEM inspections on the PAA structures are shown in fig. 6.4, these structures are made at 150 V anodization voltage. Panel a) shows a top-view image, the pores sizes vary considerably, the average pore size is ca. 200 nm. The pore distribution is not very regular. Figure 6.4b shows the cross-section of a partly anodized Al layer. Around half of the layer is converted,

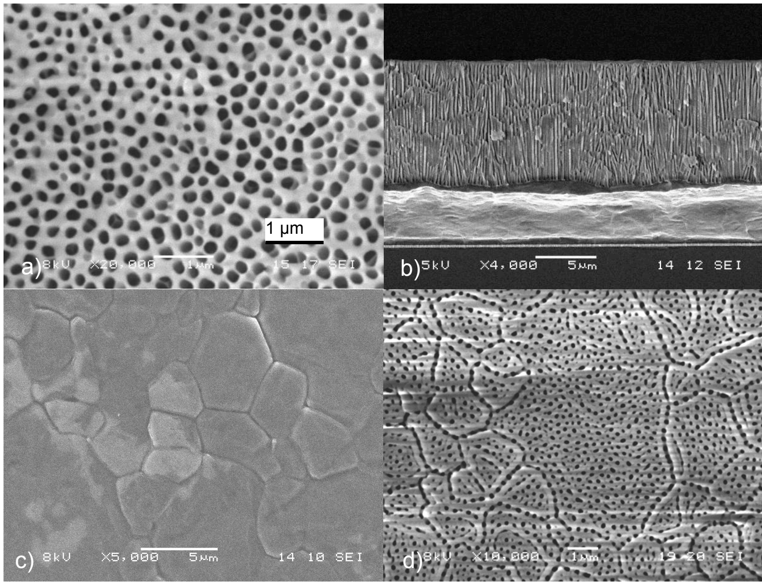

Figure 6.4 *– SEM images of PAA structures, made in 3 wt% phosphoric acid with an anodization voltage of 150 V. a) Top-view image showing the pore structure. b) Cross-section image of a partly anodized 10 μm thick Al layer. c) Top-view image of a 10 μm thick Al layer after sputtering showing the grain structure. d) Top-view image of a PAA structure where the influence of roughness is particularly severe. The grain boundaries attract more pores, creating the perforated borders.*

the PAA layer becomes ca. 40% thicker than the original Al layer.

The irregularity in the pore shape, size and distribution are related to the roughness and the grains of the Al layer. The Al layers are made by sputtering. The tools that are used for this do not have backside cooling or other facilities to prevent the layers from heating up, the result is shown in fig. 6.4c. For thick layers ($> 5\ \mu$m) the heating is so severe that it causes extensive roughening. When these layers are used for anodization the PAA appears as in fig. 6.4d.

Attempts to increase the pore pitch and pore size were not successful. Increasing the bias voltage leads to current instability. A breakdown-like event typically occurs somewhere on the Al layer. This results in excessive heating of the electrolyte. The setup that is used does not have thermostatic control of the temperature, it is intended for low voltage operation [141]. The low voltage results in narrow pores. These structures are used as a template for nanowires [142] or as a self-organized etch mask with small, sub-lithographic, features [143].

The compound sub-electrode beneath the PAA

The PAA structure cannot be directly integrated. To prevent the anodization process from running through the bondpads (that also consist of Al) a dedicated stopping layer is needed that does not react during anodization. This layer has to be conductive, it also acts as a good electrode so that all of the Al over the whole surface can be converted and no un-reacted pockets of Al are left behind. In fig. 6.4b) it can already be seen that the anodization front is not completely flat, there is a variation in conversion rate. For this reason a thin W-Ti layer (150 nm, 15 at% Ti) is deposited before the thick Al. The W-Ti layer is compatible with existing processing, it has good sheet resistance (0.4 $\Omega/\Box$) and it improves adhesion. The W-Ti can be seen in the cross-section image in fig. 6.4b, just above the scale bar.

During anodization a continuous sub-electrode is essential. But if this layer remains after the process is completed it shorts all of the pixels on the chip rendering it useless. The lateral connections need to be removed. Conventional patterning techniques, such as lithography, are not feasible because the W-Ti is covered by the very thick PAA layer. The solution to this is to provide the information on where to etch the W-Ti in a hard-mask layer below the porous alumina. This mask is already deposited and patterned before Al deposition. The process for this is shown in fig. 6.5.

The mask that is used is a thin layer of Ni, this metal is non-reactive (in the atmosphere), provides good adhesion for the Al, it also protects the W-Ti (specifically the Ti) from oxidation. The Ni is patterned to cover the Al anode pads, with a small overlap. This is shown in fig. 6.5b. After this the thick Al layer is deposited. The Al is then converted into porous alumina by anodization, this process stops on the Ni on W-Ti stack. Then the exposed W-Ti is patterned through the PAA structure with a selective wet etch. After this there is still a conductive path from the bottom of the MCP to the anode plane, while the pixels are not shorted.

The process flow described above has not been validated due to time constraints and the lack of resources. Preliminary etch selectivity tests were successful, leaving the experimental work open for continuation.

6.3 SU-8 MCP structures

There are a lot of publications focusing on the use of SU-8 for High Aspect-Ratio (HAR) structures made with lithography [76]. Many of these are dark-field structures where most of the SU-8 is removed leaving only narrow long pillars and other structures. For Light-Field structures (narrow holes in an SU-8 field) the AR limits that have been demonstrated vary between 10:1 [144] up to 20:1 [145]. Although these values may be even further improved it is hard to imagine that SU-8 can be patterned leaving 100:1 or even 50:1 holes in a single layer. This means it will

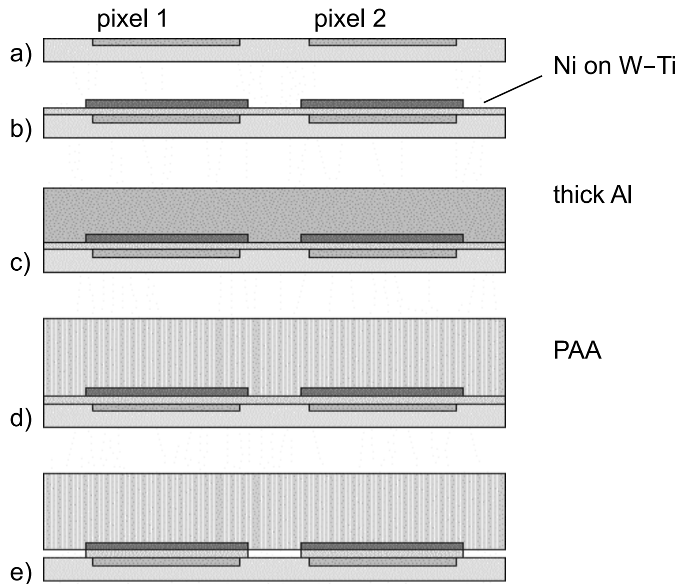

Figure 6.5 *– Process flow for the integration of a self-aligned sub-electrode. a) Starting situation b) Deposition of W-Ti, deposition and patterning of a Ni pad. c) Deposition of thick Al. d) Conversion of Al into PAA. e) Selective wet etching of the W-Ti.*

be impossible to operate a lithographically defined SU-8 MCP with high enough gain.

Improving the aspect ratio of holes in SU-8

There are two steps in the lithographic process for light-field SU-8 processing that limit the AR of holes; the exposure and the development step.

The exposure dose is calculated to provide adequate cross-linking across the entire layer. Reflections near the top surface can lead to increased cross-linking, as a result the hole becomes narrower, this is known as T-topping. In the extreme case the hole is closed off completely. Mechanisms to prevent this are an increased exposure dose, better elimination of mask-to-substrate gaps and the use of dedicated anti-reflective layers.

During the development step the unexposed, solvable, SU-8 is transported out of the holes by the developer solvent. In very narrow holes the material transport is limited by diffusion. This limits the maximum achievable AR. Methods to improve the performance include ultrasonic agitation and increased temperature of the developer.

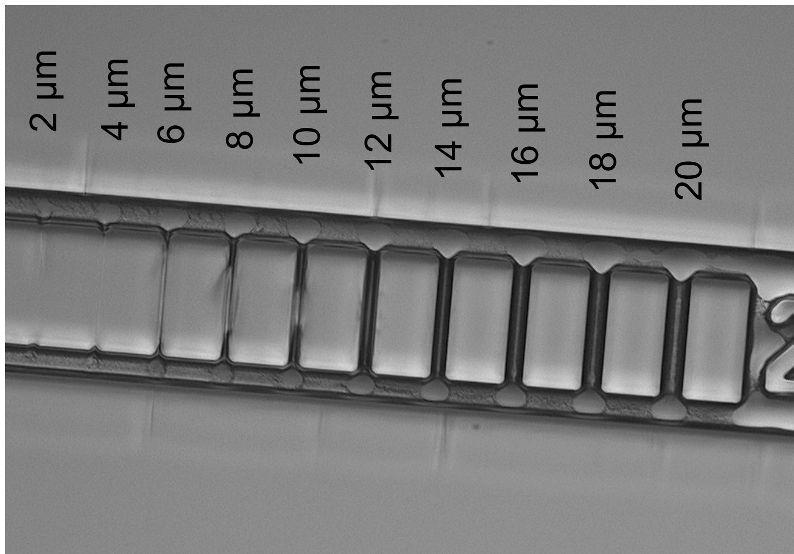

Figure 6.6 – *Top-view micrograph of a patterned SU-8 layer of 50 μm. The mask has slits of varying width, as indicated.*

Experimental results

Figure 6.6 shows the result of conventional SU-8 development in a PGMEA puddle development setup, this is the default process in the MESA+ cleanroom. The widest slits are more or less developed correctly. But starting from 10 μm the structure is not properly developed. This corresponds to an aspect-ratio of 5.

One method to improve the aspect ratio that can be achieved with SU-8 is to decrease the exposure dose by about 20% (with respect to the processing guidelines of the manufacturer). Figure 6.7 shows a pore structure that has been obtained with a thick SU-8 layer. The exposure dose that was used for these holes was 340 mJ/cm^2. The rest of the processing was conventional. The obtained pores have an aspect ratio of around 10.

Another method to improve the aspect ratio that has been tried experimentally is to define porous SU-8 structures in multiple layers. A first layer is made normally, including the development step. After that a layer of solid SU-8 foil material is applied over the structure. This laminate covers the pores. On top of the foil another normal liquid SU-8 is applied. The two new SU-8 layers are exposed and developed together. This process could possibly be repeated, although misalignment and the formation of bubbles did present difficulties during processing. Figure 6.8 shows an example of a two layer structure. The bottom layer is 100 μm thick. The second stage is made with a 20 μm foil and another 100 μm

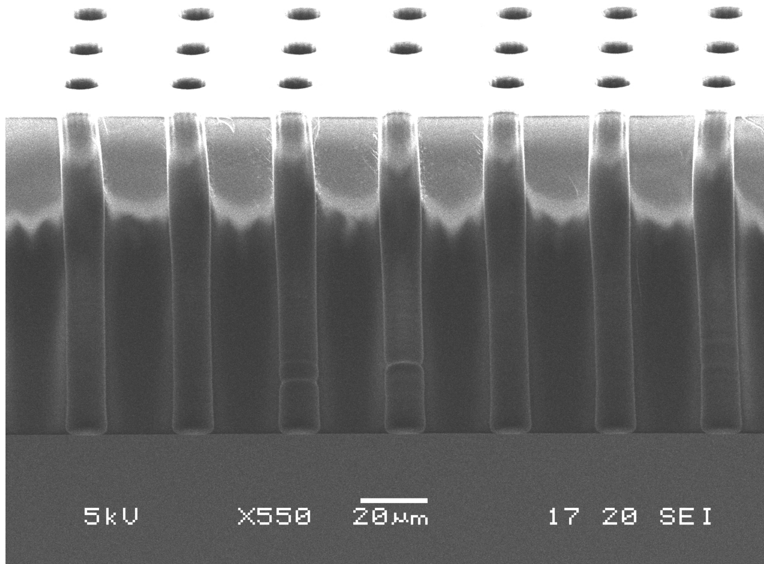

Figure 6.7 *– Cross-section SEM image of a thick SU-8 layer with a reduced exposure dose (340 mJ/cm^2).*

conventional SU-8 layer. The SU-8 foil material is made out of solid SU-8 photoresist. The sheets that we used were A4 sized trial products from Microchem Corp., currently a similar product is available from Dupont[1]. More details can be found in [146].

6.4 Conclusions

A model of MCPs has been presented. The model indicates that MCPs can be scaled, the gain process depends on first instance on the diameter to length ratio of the pores. However, the bias voltage that is needed does not scale. The energy requirement to support the growing charge cloud remains constant, it is independent of the distance over which the growth takes place.

For smaller, thinner MCPs the dielectric strength of the material used for the porous matrix needs to be considered. Gain saturation, caused by charge crowding, forms another limit. For a minimum gain of 1000 the pores need to be wider than 10 nm. A true Nano Channel Plate is not feasible.

The dielectric strength of porous Al_2O_3 appears to be sufficient. A CMOS compatible process to make anodic alumina structures has been investigated, a

[1]DuPont PerMX Series

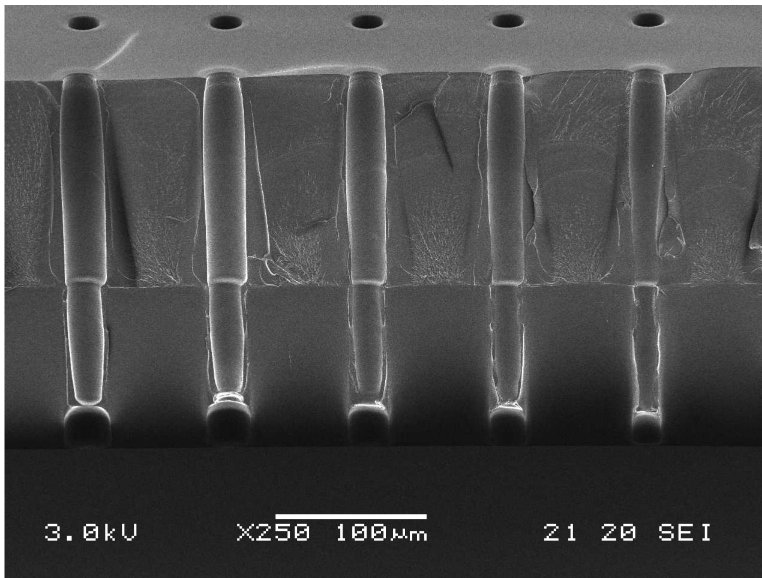

***Figure 6.8** – Cross-section SEM image of a two layer SU-8 structure*

process flow is presented. The experiments were aimed at defining structures with pore size of 0.5–1 μm. This was not realizable with the available equipment. The structures that have been made had too narrow pore width. It was not possible to increase the pore size due to current instabilities. With a different experimental setup, with better control over temperature and bias, it might become possible.

Another option is to not use the pores of the PAA directly but etch larger pores into the PAA material. The porosity of the structure can result in very good anisotropy of the etching process. During the etching process only the thin walls between pores needs to be removed. The meta pore structure that is fabricated in the PAA material can be used as an MCP structure. This has been shown before by a group of the Belarus Academy of Sciences [130, 131] for separate MCP structures, it is interesting to see if such a structure can be post-processed on a CMOS readout plane.

SU-8 has also been considered as a material for an MCP. The DS of SU-8 is found to be more than sufficient. High Aspect Ratio (HAR) structures have been demonstrated in literature although mostly on dark-field (freestanding) structures. The maximum AR that can be achieved is limited by exposure and by development. A method to increase the aspect ratio of narrow holes in SU-8 has been presented. It involves stacking layers of SU-8 that are developed individually, by separating them with SU-8 foil material.

Conclusions and recommendations

Conclusions

Post-processing of CMOS substrates is a powerful concept. Using relatively simple and cost-effective techniques standard CMOS ICs can acquire additional functionality. In this thesis we have focused on making CMOS imaging arrays able to detect other types of radiation. We have presented the InGrid device, an existing design of a gaseous detector sensitive to single electron signals. This detector was originally constructed to record ionizing radiation by detection of single electron charges created in the gas volume above the grid. The present research is aimed at exploring the use of the device to detect photoelectrons originating from the grid and thereby allow photon imaging. The design of the detector was optimized and we have performed the first experiments on photon imaging. By adding a CsI reflective photocathode the sensitivity for UV photons is greatly improved. The detector is capable of imaging UV light with a very high sensitivity and high resolution.

The InGrid structure, an integrated Micromegas device, is compatible with the additional post-processing needed for the photocathode. Also the CMOS IC has not been impacted. The resulting detector has been operated in a range of gas mixtures. Initial experiments on single anode devices, with Ar based mixtures, proved promising. These results could not be reproduced with the devices built onto Timepix substrates due to the (early) onset of discharges, before sufficient gain is achieved. For this reason most further experiments have been made with He-isobutane mixtures. This method allows higher bias voltages; it results in very stable operation. No degradation of the devices has been observed after weeks of experimenting with the same device.

The dielectric strength of SU-8 has been investigated quantitatively. It is the first time such a report is published in literature. The DS of SU-8 is determined to be 4.43 MV/cm (or 443 V/μm). This value is remarkably high for a polymer

material, it is more than sufficient for the requirements of gaseous radiation detectors. The conduction mechanism through SU-8 layers has been investigated: low field conduction stems from thermionic emission.

Outgassing from SU-8 has been characterized. The main constituents of the outgassed material can be directly linked to the resist formulation. Overall outgassing levels of cured and hard-baked SU-8 are comparable to Kapton.

The MCP model indicates that it is possible to manufacture an MCP electron multiplier directly onto CMOS substrates. Initial experiments and a proposed process flow are presented. Two methods for making a porous structure have been investigated. As it stands, the PAA structures have too narrow pores (too high aspect ratio) and the SU-8 structures have too large pores (for their thickness, *i.e.* a too low aspect ratio).

Recommendations

This thesis presents the initial results obtained with InGrid detectors coupled to photocathodes. Many things are left unexplored. The most important thing is to establish the quantum efficiency of the device in a quantitative manner. This can be done by carefully comparing the performance of the device under controlled circumstances with that of a fully characterized reference device. The device geometry and the applied bias voltage play an important role in the way (primary) electrons are transferred. More detailed analysis on a range of devices, with a variation in device geometry (*e.g.* the hole pitch of the grid) is important. Such an exercise would benefit from a more reliable and quicker manufacturing method. An effort is underway to process InGrid devices on waferscale.

An elegant way to provide a proof of single photon sensitivity and of quantum efficiency is to provide the detector, specifically the photocathode, with a single photon light source with a known flux. One such method would be to integrate a Čerenkov radiator into the detector housing. By irradiating the radiator with ionizing radiation a cone of single photons is emitted, at a known rate, that can be imaged by the detector. A suitable radiator would be NaF.

In He-isobutane the extraction level is limited to 50%. To improve the extraction level the spark protection of the device needs to be improved. This would allow a wider range of gases to be used. Further studies on the effectiveness of spark protection on the anode are underway. A recent publication presents results of this work [115]. Other methods of spark protection that are interesting to investigate would be the use of a resistive layer on the other electrode, the grid. The entire grid could be made out of a material with low conductivity, such as Si. This requires extensive technological experiments. Finally, to decrease the spark probability rather than to reduce the impact, a multistage structure such as TwinGrid

could be used. In a double stage InGrid the multiplication process can be spread across the two layers. Initial double stage devices have been made, but their use in spark prevention, and the methods of operation needed for that, have not been investigated experimentally.

This thesis presents a device with a CsI photocathode. This material is very robust, it allows easy manipulation and transfer of the device between the CsI deposition system and the measurement chamber. But the photocathode is only sensitive to a relatively narrow band of deep UV photons. To increase the range of wavelengths that can be detected other photocathodes are needed. For visible light promising results have been achieved with gaseous detectors coupled to alkali-antimonide photocathodes [122]. These are however, very delicate. Much more complicated methods are needed to handle and operate the device. Also the present Ion Back Flow (IBF) rate (2%, fig. 5.9) presents problems for the lifetime of such a device. To secure sufficient performance it is needed to lower the IBF. This requires a more detailed investigation into the IBF process in this device, with a focus on the influence of geometry and biasing. An additional method to lower IBF that could be pursued is the use of the aforementioned double stage structure.

CsI has a high resistivity. It is interesting to see if the CsI can be used not only as a photocathode but also as a resistive electrode for an InGrid device. The support structure (the pillars and the grid) could then be fully dielectric, made out of SU-8 or out of ceramic materials. The structure would be inherently spark protected as well as photosensitive.

Concerning the outgassing, it has been found that quantitative measurements are hard to do and the interpretation is also not easy. A more effective method is perhaps to investigate it in a qualitative manner. Similar to the work of Andersson *et al.* [99, 100], a long term comparative study can be made using a range of devices made out of different materials and with different treatments (*i.e.* Hard-Bake steps).

The MCP investigation presented in this thesis is entirely preliminary. The method of making porous structures needs to be studied in more detail. The anodization of Al to make an MCP requires more control over process parameters such as temperature and current. Another option would be to etch pores into an already porous material such as PAA. The directionality built into the material would significantly improve the etch anisotropy that can be attained. Concerning SU-8 porous structures it is interesting to further develop the technology of layer stacking using foil material. Another approach is to increase the aspect ratio that can be achieved in a single layer of conventional liquid SU-8. Methods that can be used include the optimization of the exposure step, such as a lower dose or further reduction of reflection around the mask-substrate gap, and of the development step, for instance by more effective agitation and possibly by development at increased temperature.

Samenvatting

Het afbeelden van fotonen met nabewerkte CMOS chips

Dit proefschrift behandelt een nieuwe manier om beeldvormende detectoren te maken voor extreem kleine hoeveelheden licht. Het uiteindelijke doel is om losse, individuele fotonen waar te nemen met een hoge resolutie. Er zijn verschillende manieren om dat te doen; in dit proefschrift behandelen we gasgevulde detectoren en vacuüm detectoren. In beide gevallen wordt het binnenkomende foton eerst omgezet in een vrij elektron met behulp van een fotokathode. Daarna worden de elektronen vermenigvuldigd. Dit gebeurt door het elektron te versnellen en te laten botsen met een atoom (bijvoorbeeld van de gasvulling), daarbij ontstaan meerdere vrije elektronen. Dit proces herhaalt zich een tiental malen langs de diepteas van de detector, de lawine van lading die hierdoor ontstaat kan waargenomen worden door een beeldgevoelige chip. Deze chip is een standaard IC ('Integrated Circuit', een geïntegreerde schakeling) van het CMOS type. Het zijn goedkoop en makkelijk te vervaardigen IC's van een wat oudere procesgeneratie. Door een uitgekiend ontwerp van het IC (dat reeds door anderen is gedaan) is de chip in staat om een lading van ongeveer 1000 elektronen goed waar te nemen.

Bovenop dit IC wordt de detectorstructuur gebouwd, we spreken van 'post-processing' of nabewerken. De hiervoor gebruikte stappen moeten zo gekozen en geoptimaliseerd worden dat het CMOS IC niet nadelig wordt beïnvloedt. De belangrijkste eis is dat de temperatuur tijdens het maken van de detectorstructuur niet boven de 450 °C komt.

Hoofdstuk 1 van dit proefschrift geeft een korte inleiding tot het onderzoeksgebied. Ook worden verschillende materialen en technieken geïntroduceerd die later gebruikt worden voor post-processing. Een van de belangrijkste materialen is SU-8, een fotogevoelig polymeer waarmee robuuste constructies gemaakt kunnen worden met behulp van fotolithografie. Dit materiaal wordt veel gebruikt, maar niet alle eigenschappen ervan zijn goed gedocumenteerd. In hoofdstuk 2 en 3 worden nieuwe experimentele resultaten gepresenteerd voor twee relevante aspecten van SU-8. Dat zijn de diëlektrische sterkte en het uitgassingsgedrag van SU-8. De conclusie van dit werk is dat SU-8 zeer geschikt is voor het door ons beoogde gebruik. De lekstromen door SU-8 worden bepaald door thermionische emissie; de diëlektrische sterkte van SU-8 is 4,43 MV/cm.

Hoofdstuk 4 behandelt het ontwerp en de vervaardiging van gasgevulde detectoren die gevoelig zijn gemaakt voor (losse) UV fotonen met behulp van fotokathodes gemaakt van CsI. Deze detectoren zijn van het zogeheten Micromegas type en bestaan uit een aluminium raster dat boven het chipoppervlak gehouden wordt door 50 μm hoge pilaartjes van SU-8.

Hoofdstuk 5 presenteert de met deze detectoren behaalde resultaten. Deze instrumenten zijn de eerste volledig geïntegreerde detectoren van dit soort. De detectoren zijn in staat om UV licht af te beelden met een uiterst hoge gevoeligheid en resolutie.

Hoofdstuk 6 ten slotte gaat over een ander soort detector, met een MCP ('Micro Channel plate') als versterkingselement. Hierbij wordt de benodigde versterking gerealiseerd door botsingen langs de wand van een dicht op elkaar gepakte structuur van lange, smalle kanalen. Het hoofdstuk behandelt methodes om zulke structuren te maken en geeft een opzet voor het maken van een op een microchip geïntegreerd detectorsysteem.

Acknowledgement

First of all I want to thank you, the reader, for your interest in this work. In this way I also hope to be able to thank those that I might have forgotten to list below.

Many people have helped in the realization of the work documented in this thesis. The first step was the decision to come to Twente and to consider a PhD in the first place. Several friends and former colleagues helped me in this, specifically I would like to thank Ray Hueting and Yukiko Furukawa. In Twente I worked together closely with my supervisors Cora Salm and Jurriaan Schmitz. I thank them for their enthusiastic support. The thesis project was part of a post-processing project. The other members were Victor Blanco Carballo, Max Chefdeville, Jiwu Lu, Erik Faber and Alexey Kovalgin. I really enjoyed working with them.

Important parts of this work have been done in the Nikhef institute in Amsterdam: thanks go to my colleagues there, Yevgen Bylevich, Martin Fransen, Max Chefdeville, Harry van der Graaf, Jan Visschers, Jan Visser, Jan Timmermans, Fred Hartjes and Joop Rövekamp.

An essential part of the thesis, the work on the photocathode integration and the validation of the resulting device, has been achieved together with Amos Breskin of the Weizmann Institute of Science (Israel) and his group. I want to thank Amos and the people I had the pleasure to work with there, Moshe Klin, Alexey Lyashenko and Marco Cortesi.

Some of the work has been done together with students, I want to thank Fleur van Rossem and Juan Carlos Villamil O. from the University of Twente. During the course of this work I received a lot of help from many people in our field, for which I am grateful. I list them here in no particular order, I sincerely hope that I did not forget anyone. Ben Hageluken from Panalytical, Teun Ruardij and André Hof from Photonis and Eugene Timmering from Philips Research. Frank Karelse from STW and the members of the STW user committee: Jan van Spijker from Photonis, Arjan Noordermeer from Panalytical, Klaus Reimann from NXP, Hans van den Vlekkert from Lionix, Erik Heijnne from CERN, Heinz Graafsma from Desy en Mart Bierhoff from FEI. The (former) MESA+ cleanroom staff: Dominique Bouwes, Ite-Jan Hoolsema, Ton Jenneboer, Peter Linders, Hans Mertens, Marion Nijhuis-Groen, Samantha Ooijman-Geerdink, Gerard Roelofs, Eddy Ruiter, Huib van Vossen, Robert Wijn, Rene Wolf. And the following colleagues from the University of Twente: Mark Smithers, Rico Keim, Raoul van

Gastel, Herbert Wormeester, Stefan Kooij and Nima Izadi.

The defense of this thesis is overseen by a committee, apart from my promotor Jurriaan Schmitz and assistent promotor Cora Salm, these people are Prof. Dr. Ir. A.J. Mouthaan (University of Twente), Prof. Dr. K. Desch (University of Bonn), Dr. Ir. H. van der Graaf (Nikhef), Prof. Dr. M.C. Elwenspoek (University of Twente), Prof. Dr. Ir. R.A.M. Wolters (University of Twente and NXP Semiconductors) and Prof. Dr. G. van der Steenhoven (University of Twente). I would like to thank them for their time and effort.

Being on floor 3 has always been good to me. I never really got used to the new building. Although I did get attached in some way to the Hogekamp it is really the people that I will miss. A special set of thanks go to Annemiek Janssen for everything she has done for me through the years. Furthermore I want to thank all my other colleagues and friends, Sander, Rob, Henk, Cora, Jurriaan, Gerard, Gerdien, Tom, Alexey, Ray, Giulia, Pietro, Guido, Jan-Laurens, Tu, Naveed, Jisk, Radko, Deepu, Fred, Phuong, Jiwu, Erik, Vidhu, Hao, Faisal, Mark, Natalie, Sumy, Arjen, Ihor, Alfons, Balaji, Faisal, Rodolf, Bijoy, Victor, Shuo, Xiaoqin, Wei, Zhiyu, Yiping, Maurizio, Boni, Buket and Tom.

I am very lucky to have two capable paranymphs during the defense: Giulia and Bijoy, thank you for your support.

Lastly I want to thank my family members and friends who have supported me throughout the years. Specifically I want to mention Hein, Marieke, Wimpie and Theo, my parents in law in Kimitsu and my wife Yukiko. Without you I would not have been able to finish this thesis.

Enschede, November 2010

About the author

Joost Melai was born on December 30, 1976, in Nijmegen, the Netherlands. After finishing secondary education at the Lorentz Lyceum in Eindhoven he moved to Enschede. In 2000 Joost obtained a B.Sc. degree in Applied Physics from the Hogeschool Enschede (this school is now called Fontys). He then took a position in Philips Research Leuven. This division was located at the site of IMEC in Leuven, Belgium and it is now part of NXP Semiconductors.

For the next 5 years he worked on bipolar device integration for advanced BiCMOS and discrete bipolar technologies. In this period he worked on the Resurf HBT together with Ray Hueting and others. This work was presented at the 2004 IEEE ISPSD, Mr. Melai and coauthors were awarded the Best Paper Award for this contribution.

In 2005 Joost joined the Semiconductor Components group, part of the Mesa+ Institute of the University of Twente in Enschede, the Netherlands. His supervisor there was Prof. Jurriaan Schmitz. From 2005 until the end of 2010 he has worked on post-processing technologies for radiation detection. The thesis you are reading is the result of the work performed in this period. Joost Melai has (co-)authored more than 16 papers and 9 patent applications.

Bibliography

[1] Press release by Canon Inc, August 31 2010, http://www.canon.com/news/2010/aug31e.html

[2] B. Burke, P. Jorden and P. Vu. *CCD technology*. Exp. Astron., 19(1–3), pp. 69–102, 2005.

[3] http://cfht.hawaii.edu/en/

[4] Z. Vykydal *et al.* *The RELAXd project: Development of four-side tilable photon-counting imagers*. Nuclear Instruments and Methods A, 591(1), pp. 241 – 244, 2008.

[5] J. Bosiers, I. Peters, C. Draijer and A. Theuwissen. *Technical challenges and recent progress in CCD imagers*. Nuclear Instruments and Methods A, 565, pp. 148–156, 2006.

[6] A. Fornaini, D. Calvet and J. L. Visschers. *Soft X-ray sensitivity of a photon-counting hybrid pixel detector with a silicon sensor matrix*. Nuclear Instruments and Methods A, 466(1), pp. 142–145, 2001.

[7] B. Mikulec. *Single Photon Detection with Semiconductor Pixel Arrays for Medical Imaging Applications*. PhD thesis, University of Vienna, Austria, 2000.

[8] G. Pellegrini *et al.* *Performance limits of a 55-m pixel CdTe detector*. IEEE Transactions on Nuclear Science, 53(1), pp. 361–6, 2006.

[9] S. M. Sze and K. K. Ng. *Physics of Semiconductor Devices*. Wiley-Interscience, Hoboken, New Jersey, USA, 3rd edition, 2007.

[10] W. Boyle and G. Smith. *The inception of charge-coupled devices*. IEEE Transactions on Electron Devices, ED-23(7), pp. 661–663, 1976.

[11] G. Hobson. *Charge-Transfer Devices*. Edward Arnold, London, 1978.

[12] http://en.wikipedia.org/wiki/Charge-coupled_device

[13] P. Jerram *et al.* *The LLLCCD: low light imaging without the need for an intensifier*. proceedings of SPIE, volume 4306, pp. 178–186, 2001.

[14] P. Holl *et al. A New High-Speed, Single Photon Imaging CCD for the Optical*. IEEE Nuclear Science Symposium Conference Record, 3, pp. 1589–1594, 2006.

[15] A. J. Theuwissen. *CMOS Image Sensors : State-of-the-art*. Solid-State Electronics, 52, pp. 1401–1406, 2008.

[16] F. Zappa, S. Tisa, A. Gulinatti, A. Gallivanoni and S. Cova. *Monolithic CMOS detector module for photon counting and picosecond timing*. proceedings of the ESSDERC, p. 341, 2004.

[17] F. Zappa, S. Tisa, A. Gulinatti, A. Gallivanoni and S. Cova. *Complete single-photon counting and timing module in a microchip*. Optics Letters, 30(11), p. 1327, 2005.

[18] W. J. Kindt, N. H. Shahrjerdy and H. W. van Zeijl. *A silicon avalanche photodiode for single optical photon counting in the Geiger mode*. Sensors and Actuators A (Physical), A60(1-3), p. 98, 1997.

[19] A. Rochas *et al.* *First fully integrated 2-D array of single-photon detectors in standard CMOS technology*. IEEE Photonics Technology Letters, 15(7), p. 963, 2003.

[20] B. Rae *et al.* *A Microsystem for Time-Resolved Fluorescence Analysis using CMOS Single-Photon Avalanche Diodes and Micro-LEDs*. proceedings of IEEE ISSCC, 2008.

[21] P. Buzhan *et al.* *Silicon photomultiplier and its possible applications*. Nuclear Instruments and Methods A, 504(1–3), pp. 48–52, 2003.

[22] G. Anelli *et al.* *A new concept of monolithic silicon pixel detectors: hydrogenated amorphous silicon on ASIC*. Nuclear Instruments and Methods A, 518(1–2), p. 366, 2004.

[23] C. Miazza *et al.* *Performance analysis of a-Si:H detectors deposited on CMOS chips*. MRS Symposium Proceedings, volume 808, p. 513, 2004.

[24] N. Moussy *et al.* *A highly reliable Amorphous Silicon photosensor for above IC CMOS image sensor*. proceedings of IEEE IEDM, 2006.

[25] O. Matsushima *et al.* *A high-sensitivity broadband image sensor using CuInGaSe2 thin films*. proceedings of IEEE IEDM, 2008.

[26] http://en.wikipedia.org/wiki/PM_tube

[27] S. Fukuda *et al.* *The Super-Kamiokande detector*. Nuclear Instruments and Methods A, 501(2–3), pp. 418–462, 2003.

[28] J. L. Wiza. *Microchannel plate detectors*. Nuclear Instruments and Methods, 162(1–3, pt.II), p. 587, 1979.

[29] P. D. Read *et al.* *Uses of microchannel plate intensified detectors for imaging applications in the X-ray, EUV and visible wavelength regions*. Nuclear Instruments and Methods A, 392(1–3), p. 359, 1997.

[30] http://www.photonis.com/industryscience/products/image_intensifiers

[31] L. Benussi *et al.* *A multichannel single-photon sensitive detector for high-energy physics: the megapixel EBCCD*. Nuclear Instruments and Methods A, 442(1–3), p. 154, 2000.

[32] C. D. D'Ambrosio *et al.* *Gamma spectroscopy and optoelectronic imaging with hybrid photon detector*. Nuclear Instruments and Methods A, 497(1), p. 186, 2003.

[33] J. Vallerga *et al.* *Optically sensitive Medipix2 detector for adaptive optics wavefront sensing*. Nuclear Instruments and Methods A, 546(1–2), p. 263, 2005.

[34] B. Mikulec *et al.* *A high resolution, high frame rate detector based on a microchannel plate readout with the Medipix2 counting CMOS pixel chip*. IEEE Trans. on Nuclear Science, 52(4), p. 1021, 2005.

[35] J. Vallerga, J. McPhate, A. Tremsin and O. Siegmund. *High-resolution UV, alpha and neutron imaging with the Timepix CMOS readout*. Nuclear Instruments and Methods A, 591(1), pp. 151–154, 2008.

[36] F. Sauli. *Principles of operation of multiwire proportional and drift chambers*. Technical report, CERN, 1977.

[37] M. Chefdeville. *Development of Micromegas-like gaseous detectors using a pixel readout chip as collecting anode*. PhD thesis, University of Amsterdam, 2008.

[38] H. Geiger and W. Müller. *Elektronenzählrohr zur Messung schwächster Aktivitäten*. Die Naturwissenschaften, 16(31), pp. 617–618, 1928.

[39] Press Release: The 1992 Nobel Prize in Physics, http://nobelprize.org/nobel_prizes/physics/laureates/1992/press.html

[40] G. Charpak, R. Bouclier, T. Bressani, J. Favier and C. Zupancic. *The use of multiwire proportional counters to select and localize charged particles*. Nuclear Instruments and Methods, 62(3), pp. 262–268, 1968.

[41] F. Sauli. *GEM: A new concept for electron amplification in gas detectors*. Nuclear Instruments and Methods A, 386(2–3), p. 531, 1997.

[42] C. Shalem, R. Chechik, A. Breskin and K. Michaeli. *Advances in Thick GEM-like gaseous electron multipliers - Part I: Atmospheric pressure operation*. Nuclear Instruments and Methods A, 558(2), p. 475, 2006.

[43] C. K. Shalem, R. Chechik, A. Breskin, K. Michaeli and N. Ben-Haim. *Advances in thick GEM-like gaseous electron multipliers Part II: Low-pressure operation*. Nuclear Instruments and Methods A, 558(2), p. 468, 2006.

[44] R. Chechik and A. Breskin. *Advances in gaseous photomultipliers*. Nuclear Instruments and Methods A, 595(1), p. 116, 2008.

[45] J. M. Bidault *et al.* *A Novel UV Photon Detector with Resistive Electrodes*. Nuclear Physics B - Proceedings Supplements, 158, p. 199, 2006.

[46] A. Di Mauro *et al.* *Development of innovative micro-pattern gaseous detectors with resistive electrodes and first results of their applications*. Nuclear Instruments and Methods A, 581(1–2), p. 225, 2007.

[47] A. V. Lyashenko *et al.* *Advances in ion back-flow reduction in cascaded gaseous electron multipliers incorporating R-MHSP elements*. Journal of Instrumentation, 1(10), p. P10004, 2006.

[48] A. V. Lyashenko *et al.* *Further progress in ion back-flow reduction with patterned gaseous hole-multipliers*. Journal of Instrumentation, 2(8), p. P08004, 2007.

[49] Y. Giomataris, P. Rebourgeard, J. P. Robert and G. Charpak. *MICROMEGAS: a high-granularity position-sensitive gaseous detector for high particle-flux environments*. Nuclear Instruments and Methods A, 376(1), p. 29, 1996.

[50] K. N. *et al.* (Particle Data Group). *The Review of Particle Physics*. Journal of Physics G: Nuclear and Particle Physics, 37(7A), p. 075021, 2010.

[51] A. Oed. *Position-sensitive detector with microstrip anode for electron multiplication with gases*. Nuclear Instruments and Methods A, A263(2–3), p. 351, 1988.

[52] T. Nagayoshi *et al.* *Development of [mu]-PIC and its imaging properties*. Nuclear Instruments and Methods A, 525(1–2), pp. 20–27, 2004.

[53] R. Bellazzini *et al.* *Reading a GEM with a VLSI pixel ASIC used as a direct charge collecting anode*. Nuclear Instruments and Methods A, 535(1–2), p. 477, 2004.

[54] R. Bellazzini *et al.* *Imaging with the invisible light*. Nuclear Instruments and Methods A, 581(1–2), p. 246, 2007.

[55] R. Bellazzini *et al.* *X-ray polarimetry with Gas Pixel Detectors: A new window on the X-ray sky*. Nuclear Instruments and Methods A, 576(1), p. 183, 2007.

[56] P. Colas *et al.* *The readout of a GEM or Micromegas-equipped TPC by means of the Medipix2 CMOS sensor as direct anode*. Nuclear Instruments and Methods A, 535(1–2), p. 506, 2004.

[57] M. Campbell *et al.* *Detection of single electrons by means of a Micromegas-covered MediPix2 pixel CMOS readout circuit*. Nuclear Instruments and Methods A, 540(2–3), p. 295, 2005.

[58] T. Tanimori, Y. Nishi, A. Ochi and Y. Nishi. *Imaging gaseous detector based on micro-processing technology*. Nuclear Instruments and Methods A, 436(1–2), p. 188, 1999.

[59] V. Peskov, E. Silin, T. Sokolova and I. Radionov. *First attempts to combine capillary tubes with photocathodes*. Nuclear Instruments and Methods A, 433(1-2), p. 492, 1999.

[60] J. Va'vra and T. Sumiyoshi. *Single electron amplification in a ""single-MCP + Micromegas + pads"" detector*. Nuclear Instruments and Methods A, 535(1–2), p. 334, 2004.

[61] J. Schmitz. *Adding functionality to microchips by wafer post-processing*. Nuclear Instruments and Methods A, 576(1), pp. 142–149, 2007.

[62] X. Llopart, M. Campbell, R. Dinapoli, D. San Segundo and E. Pernigotti. *Medipix2: A 64-k pixel readout chip with 55- mu m square elements working in single photon counting mode*. IEEE Transactions on Nuclear Science, 49(5, pt.1), p. 2279, 2002.

[63] X. Llopart, R. Ballabriga, M. Campbell, L. Tlustos and W. Wong. *Timepix, a 65k programmable pixel readout chip for arrival time, energy and/or photon*

counting measurements. Nuclear Instruments and Methods A, 581(1–2), p. 485, 2007.

[64] X. Llopart, R. Ballabriga, M. Campbell, L. Tlustos and W. Wong. *Erratum to "Timepix, a 65 k programmable pixel readout chip for arrival time, energy and/or photon counting measurements" [Nucl. Instr. and Meth. A. 581 (2007) 485–494]*. Nuclear Instruments and Methods A, 585(1), p. 106, 2008.

[65] http://medipix.web.cern.ch/MEDIPIX/

[66] A. Fornaini. *X-ray imaging and readout of a TPC with the Medipix CMOS ASIC*. PhD thesis, University of Twente, 2005.

[67] V. M. Blanco Carballo. *Radiation Imaging Detectors Made by Wafer Post-processing of CMOS chips*. PhD thesis, University of Twente, 2009.

[68] V. M. Blanco Carballo *et al. A radiation imaging detector made by postprocessing a standard CMOS chip*. IEEE Electron Device Letters, 29(6), p. 585, 2008.

[69] M. Chefdeville *et al. An electron-multiplying 'Micromegas' grid made in silicon wafer post-processing technology*. Nuclear Instruments and Methods A, 556(2), p. 490, 2006.

[70] H. Lorenz *et al. SU-8: a low-cost negative resist for MEMS*. Journal of Micromechanics and Microengineering, 7, p. 121, 1997.

[71] http://www.microchem.com/products/su_eight.htm

[72] P. M. Dentinger, W. M. Clift and S. H. Goods. *Removal of SU-8 photoresist for thick film applications*. Microelectronic Engineering, 61–62, p. 993, 2002.

[73] S.-J. Kim, H. Yang, K. Kim, Y. T. Lim and H.-B. Pyo. *Study of SU-8 to make a Ni master-mold: adhesion, sidewall profile, and removal*. Electrophoresis, 27(16), p. 3284, 2006.

[74] C. H. Lee and K. Jiang. *Fabrication of thick electroforming micro mould using a KMPR negative tone photoresist*. Journal of Micromechanics and Microengineering, 18(5), p. 055032, 2008.

[75] H. Sato, H. Matsumura, S. Keino and S. Shoji. *An all SU-8 microfluidic chip with built-in 3D fine microstructures*. Journal of Micromechanics and Microengineering, 16(11), p. 2318, 2006.

[76] A. del Campo and C. Greiner. *SU-8: a photoresist for high-aspect-ratio and 3D submicron lithography*. Journal of Micromechanics and Microengineering, 17(6), pp. R81–R95, 2007.

[77] S. Bystrova, R. Luttge and A. van den Berg. *Study of crack formation in high-aspect ratio SU-8 structures on silicon*. Microelectronic Engineering, 84(5–8), p. 1113, 2007.

[78] T. Pan, A. Baldi and B. Ziaie. *Remotely adjustable check-valves with an electrochemical release mechanism for implantable biomedical microsystems*. Biomedical Microdevices, 9(3), p. 385, 2007.

[79] C. Salm, V. M. Blanco Carballo, J. Melai and J. Schmitz. *Reliability aspects of a radiation detector fabricated by post-processing a standard CMOS chip*. Microelectronics Reliability, 48(8–9), p. 1139, 2008.

[80] H. Lorenz, M. Laudon and P. Renaud. *Mechanical characterization of a new high-aspect-ratio near UV-photoresist*. Microelectronic Engineering, 41–42, p. 371, 1998.

[81] E. H. Conradie and D. F. Moore. *SU-8 thick photoresist processing as a functional material for MEMS applications*. Journal of Micromechanics and Microengineering, 12, p. 368, 2002.

[82] H. Yu, O. Balogun, B. Li, T. W. Murray and X. Zhang. *Fabrication of three-dimensional microstructures based on singled-layered SU-8 for lab-on-chip applications*. Sensors and Actuators, A: Physical, 127(2), p. 228, 2006.

[83] H. S. Khoo, K. K. Liu and F. G. Tseng. *Mechanical strength and interfacial failure analysis of cantilevered SU-8 microposts*. Journal of Micromechanics and Microengineering, 13(6), p. 822, 2003.

[84] R. Feng and R. J. Farris. *Influence of processing conditions on the thermal and mechanical properties of SU8 negative photoresist coatings*. Journal of Micromechanics and Microengineering, 13(1), p. 80, 2003.

[85] J. Hammacher *et al.* *Stress engineering and mechanical properties of SU-8-layers for mechanical applications*. Microsystem Technologies, 14(9–11), p. 1515, 2008.

[86] M. J. Key, V. Cindro and M. Lozano. *On the radiation tolerance of SU-8, a new material for gaseous microstructure radiation detector fabrication*. Radiation Physics and Chemistry, 71(5), p. 1003, 2004.

[87] J. R. Thorpe, J. R. Thorpe, D. P. Steenson and R. E. Miles. *High frequency transmission line using micromachined polymer dielectric High frequency transmission line using micromachined polymer dielectric*. Electronics Letters, 34(12), p. 1237, 1998.

[88] I.-H. Song and P. Ajmera. *Use of a photoresist sacrificial layer with SU-8 electroplating mould in MEMS fabrication*. Journal of Micromechanics and Microengineering, 13(6), pp. 816–21, 2003.

[89] A. Hartley, R. Miles, N. Dimitrakopoulos and D. Pollard. *SU-8 Beams and Membranes*. proceedings of EMRS DTC, p. A11, 2004.

[90] J. Melai *et al.* *Considerations on using SU-8 as a construction material for high aspect ratio structures*. proceedings of the STW SAFE workshop, pp. 529–534, 2007.

[91] J. Melai, C. Salm, S. Smits, J. Visschers and J. Schmitz. *The electrical conduction and dielectric strength of SU-8*. Journal of Micromechanics and Microengineering, 19(6), p. 065012, 2009.

[92] S. Wolf and R. N. Tauber. *Silicon Processing for the VLSI era, Volume 1 - Process Technology*. Latice Press, Sunset Beach, CA, USA, 1986.

[93] S. M. Sze and K. K. Ng. *Physics of Semiconductor Devices*, pp. 157, 227–228. Wiley-Interscience, Hoboken, New Jersey, 3rd edition, 2007.

[94] http://www2.dupont.com/Kapton/en_US/products/index.html

[95] J. Suthar *et al.* *Evaluation of dielectric films for aerospace and space power wiring insulation*. proceedings of IEEE Int. Symp. on Electrical Insulation, pp. 17–20, 1992.

[96] http://www.paryleneinc.com/pdf/PDS_Dimer_International.pdf

[97] T. Giants. *Crystallinity and dielectric properties of PEEK, poly(ether ether ketone)*. IEEE Transactions on Dielectrics and Electrical Insulation, 1(6), pp. 991–999, 1994.

[98] M. B. Chan-Park, Z. Jun, Y. Yehai and C. Y. Yue. *Fabrication of large SU-8 mold with high aspect ratio microchannels by UV exposure dose reduction*. Sensors and Actuators B (Chemical), B101(1–2), p. 175, 2004.

[99] H. Andersson *et al.* *Analysis of compounds released from various detector materials and their impact on aging characteristics of proportional counters*. IEEE Transactions on Nuclear Science, 51(5 pt.I), pp. 2110–2118, 2004.

[100] H. Andersson *et al. Aging of proportional counters with gas mixtures containing impurities of aromatic hydrocarbons*. IEEE Nuclear Science Symposium Conference Record, pp. 2053–2057. 2004.

[101] N. Kato, C. S. Park, T. Matsumoto, H. Kikuta and K. Iwata. *Fabrication of polymer cantilevers for force controlled atomic force microscope*. proceedings of SPIE, volume 5183, p. 71, 2003.

[102] Y. K. Kim, S. H. Yi, S. W. Kim and B. K. Ju. *A novel low-temperature microcap packaging using SU-8 bonding*. proceedings of IEEE Transducers '07 and Eurosensors XXI, p. 2107, 2007.

[103] D. Sameoto, S. W. Lee and M. Parameswaran. *Electrical interconnection through optimized wirebonding onto SU-8 structures and actuators*. Journal of Micromechanics and Microengineering, 18(7), p. 075023, 2008.

[104] J. K. Chen *et al. Fabrication of curved structures with electron-beam and surface structure characterization*. Journal Of Vacuum Science and Technology B, 22(2), pp. 492–500, 2004.

[105] Private communications with B. Hageluken (Panalytical Eindhoven, NL).

[106] J. F. O'Hanlon. *A user's guide to vacuum technology*. Wiley Interscience, Hoboken, NJ, USA, 3rd edition, 2003.

[107] R. N. Peacock. *Practical selection of elastomer materials for vacuum seals*. Journal of Vacuum Science and Technology, 17, p. 330, 1980.

[108] A. Breskin *et al. Sealed GEM photomultiplier with a CsI photocathode: ion feedback and ageing*. Nuclear Instruments and Methods A, 478(1–2), p. 225, 2002.

[109] D. Mörmann. *Study of novel gaseous photomultipliers for UV and visible light*. PhD thesis, Weizmann Institute of Science, Israel, 2005.

[110] J. Melai *et al. An integrated Micromegas UV-photon detector*, submitted to Nuclear Instruments and Methods A http://arxiv.org/abs/1003.1971v1, 2010.

[111] J. Melai *et al. A UV Sensitive Integrated Micromegas with Timepix Readout*, submitted to Nuclear Instruments and Methods A http://arxiv.org/abs/1003.2083v1, 2010

[112] A. Breskin. *CsI UV photocathodes: history and mystery*. Nuclear Instruments and Methods A, 371(1–2), pp. 116–36, 1996.

[113] J. Derré *et al. Fast signals and single electron detection with a MICROMEGAS photodetector*. Nuclear Instruments and Methods A, 449(1–2), p. 314, 2000.

[114] J. Jakubek *et al. Pixel detectors for imaging with heavy charged particles*. Nuclear Instruments and Methods A, 591(1), pp. 155–158, 2008.

[115] Y. Bilevych *et al. Spark protection layers for CMOS pixel anode chips in MPGDs*. to be published in Nuclear. Instruments and Methods A.

[116] L. Coelho *et al. Measurement of the photoelectron-collection efficiency in noble gases and methane*. Nuclear Instrum. and Methods A, 581(1–2), pp. 190–193, 2007.

[117] J. Escada *et al. Measurements of photoelectron extraction efficiency from CsI into mixtures of Ne with CH 4 , CF 4 , CO 2 and N 2*. Journal of Instrumentation, 4(11), p. P11025, 2009.

[118] Comsol. *COMSOL Multiphysics*, 2009.

[119] T. Holy *et al. Data acquisition and processing software package for Medipix2*. Nuclear Instruments and Methods A, 563(1), p. 254, 2006.

[120] A. Tremsin, S. Ruvimov and O. Siegmund. *Structural transformation of CsI thin film photocathodes under exposure to air and UV irradiation*. Nuclear Instruments and Methods A, 447(3), p. 614, 2000.

[121] V. I. Razin, Y. N. Gotovcev, A. B. Kurepin and A. I. Reshetin. *The influence of exposure to air on the quantum efficiency of thin CsI photocathodes*. Nuclear Instruments and Methods A, 419, p. 621, 1998.

[122] A. V. Lyashenko *et al. Development of high-gain gaseous photomultipliers for the visible spectral range*. Journal of Instrumentation, 4(7), p. P07005, 2009.

[123] P. D. Burns and D. Williams. *Using Slanted Edge Analysis for Color Registration Measurement*. Proceedings PICS Conference (Imaging Science and Technology), pp. 51–53, 1999.

[124] C. P. Beetz, R. Boerstler, J. Steinbeck, B. Lemieux and D. R. Winn. *Silicon-micromachined microchannel plates*. Nuclear Instruments and Methods A, 442(1–3), p. 443, 2000.

[125] O. H. W. Siegmund, A. S. Tremsin and J. V. Vallerga. *Advanced MCP sensors for UV/visible astronomy and biology*. Nuclear Instruments and Methods A, 510(1–2), p. 185, 2003.

[126] D. Beaulieu *et al. Nano-engineered ultra-high-gain microchannel plates*. Nuclear Instruments and Methods A, 607(1), pp. 81–84, 2009.

[127] E. H. Eberhardt. *Gain model for microchannel plates*. Applied Optics, 18(9), p. 1418, 1979.

[128] A. P. Li, F. Muller and U. Gosele. *Polycrystalline and monocrystalline pore arrays with large interpore distance in anodic alumina*. Electrochemical and Solid-State Letters, 3(3), p. 131, 2000.

[129] M. Yoshimura and H. K. Bowen. *Electrical breakdown strength of alumina and high temperatures*. Journal of the American Ceramic Society, 64(7), p. 404, 1981.

[130] K. Delendik, I. Emeliantchik, A. Litomin, V. Rumyantsev and O. Voitik. *Aluminium oxide microchannel plates*. Nuclear Physics B, Proc. Suppl., 125, p. 394, 2003.

[131] A. Govyadinov, I. Emeliantchik and A. Kurilin. *Anodic aluminum oxide microchannel plates*. Nuclear Instruments and Methods A, 419(2–3), p. 667, 1998.

[132] Y. Whikun *et al. Novel fabrication method of microchannel plates*. Review of Scientific Instruments, 71(11), p. 4165, 2000.

[133] Y. Whikun *et al. Characteristic features of new electron-multiplying channels in a field emission display*. Journal of Vacuum Science and Technology B (Microelectronics and Nanometer Structures), 19(6), p. 2247, 2001.

[134] J. O'Sullivan and G. Wood. *The Morphology and Mechanism of Formation of Porous Anodic Films on Aluminium*. Proceedings of the Royal Society of London, Series A, Mathematical and Physical Sciences, 317(1531), pp. 511–543, 1970.

[135] H. Masuda and K. Fukuda. *Ordered metal nanohole arrays made by a two-step replication of honeycomb structures of anodic alumina*. Science, 268(5216), p. 1466, 1995.

[136] H. Masuda, F. Hasegwa and S. Ono. *Self-ordering of cell arrangement of anodic porous alumina formed in sulfuric acid solution*. Journal of the Electrochemical Society, 144(5), p. 127, 1997.

[137] H. Masuda *et al. Highly ordered nanochannel-array architecture in anodic alumina*. Applied Physics Letters, 71(19), p. 2770, 1997.

[138] H. Masuda, K. Yada and A. Osaka. *Self-ordering of cell configuration of anodic porous alumina with large-size pores in phosphoric acid solution*. Japanese Journal of Applied Physics, Part 2 (Letters), 37(11A), p. 1340, 1998.

[139] A. P. Li, F. Muller, A. Birner, K. Nielsch and U. Gosele. *Hexagonal pore arrays with a 50-420 nm interpore distance formed by self-organization in anodic alumina*. Journal of Applied Physics, 84(11), p. 6023, 1998.

[140] A.-P. Li, F. Muller, A. Birner, K. Nielsch and U. Gosele. *Fabrication and microstructuring of hexagonally ordered two-dimensional nanopore arrays in anodic alumina*. Advanced Materials, 11(6), p. 483, 1999.

[141] A. C. Galca *et al. Structural and optical characterization of porous anodic aluminum oxide*. Journal of Applied Physics, 94(7), p. 4296, 2003.

[142] O. Rabin *et al. Formation of thick porous anodic alumina films and nanowire arrays on silicon wafers and glass*. Advanced Functional Materials, 13(8), p. 631, 2003.

[143] H. Asoh, K. Sasaki and S. Ono. *Electrochemical etching of silicon through anodic porous alumina*. Electrochemistry Communications, 7(9), p. 953, 2005.

[144] T. A. Anhoj, A. M. Jorgensen, D. A. Zauner and J. Hubner. *The effect of soft bake temperature on the polymerization of SU-8 photoresist*. Journal of Micromechanics and Microengineering, 16(9), p. 1819, 2006.

[145] J. Zhang, M. B. Chan-Park, M. Jianmin and T. T. Sun. *Reduction of diffraction effect for fabrication of very high aspect ratio microchannels in SU-8 over large area by soft cushion technology*. Microsystem Technologies, 11(7), p. 519, 2005.

[146] J. Melai, V. M. Blanco Carballo, C. Salm and J. Schmitz. *Suspended membranes, cantilevers and beams using SU-8 foils*. Microelectronic Engineering, 87(5–8), pp. 1274–1277, 2010.